PET ENGINEERING COLLEGE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

UNIT – III

SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES

CLASS : S5 ECE

SUBJECT CODE : EC3552

SUBJECT NAME : VLSI AND CHIP DESIGN

REGULATION : 2021

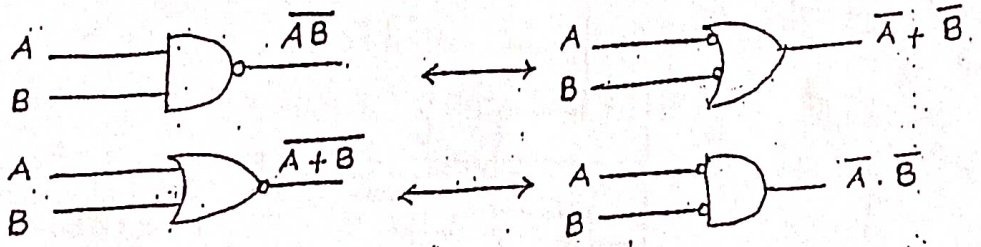
CIRCUIT FAMILIES

* Alternative CMOS Logic configurations can be called as circuit families.

Static CMOS :-

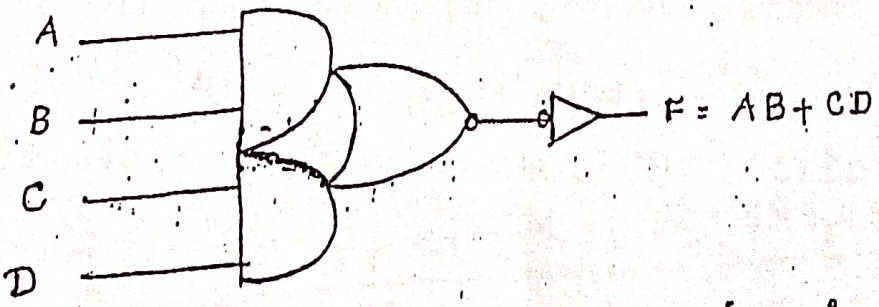
① Bubble pushing

* CMOS stages are inherently inverting. so AND and OR functions must be built from NAND and NOR gates.
* NAND gate is equivalent to an OR of inverted inputs.
* NOR gate is equivalent to an AND of inverted inputs.
* switching between these representations is easy to do on a white board and is often called bubble pushing.

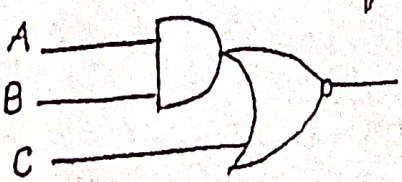


② Compound Gates

* The function $AB+CD$ can be computed with an AND-OR-INVERTER 22 (AOI 22) gate and an inverter.



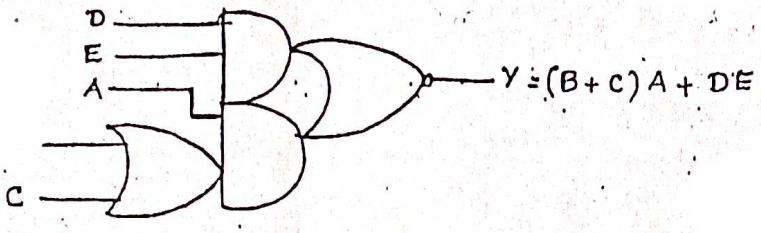
* The transistor widths are chosen to give the same drive as a unit inverter.



AOI 21

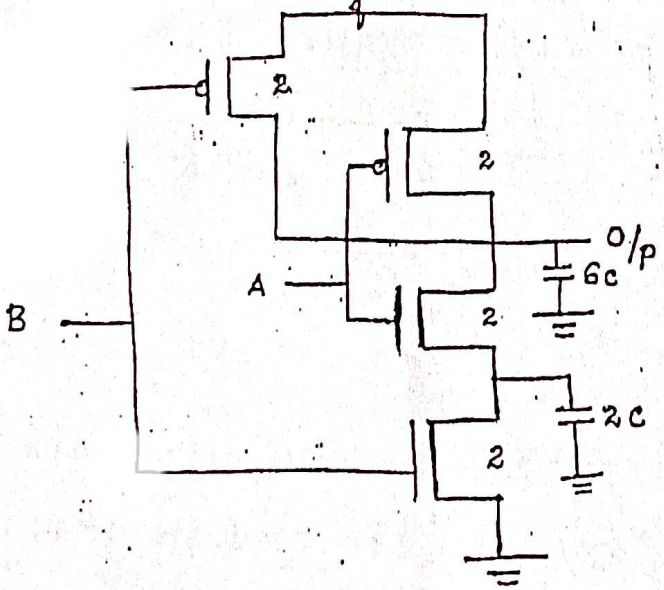
$F = \overline{AB+C}$

1. Complex AOI



(3) Input ordering Delay effect :-

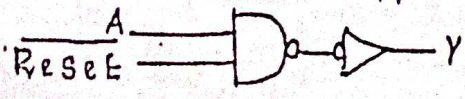
* The logic effort and parasitic delay of different ate input is often different.
* The outer input to be the input closer to the supply (i/p B) and the inner input to be the input closer to output (i/p A)
* The parasitic delay is smaller when the inner i/p switches last because the intermediate nodes have already been discharged.



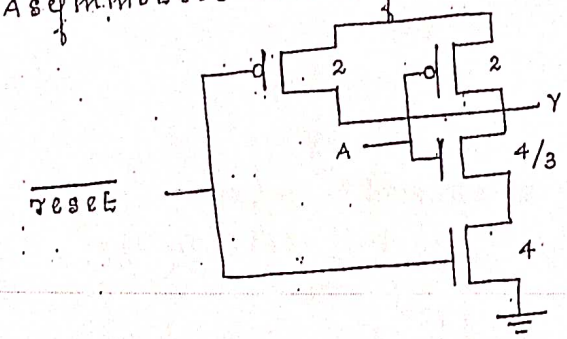
NAND gate delay estimation

(4) Asymetric Gates :-

* When one input is far less critical than another, symmetric gates can be made asymmetric to favor the late i/p.
* Consider the input reset is slow, the circuit should be optimized for i/p to o/p delay in the expense of reset.



Asymmetric NAND gate



* Pull down resistance = $R/4 + R/4/3 = R$

  Capacitance at A = 10/3

  Logical effort g_A = 10/9

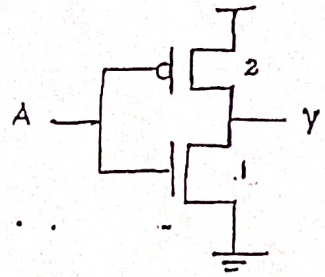
* This g_A is better than the logical effort of ordinary NAND gate.

(5) Skewed Gates :-

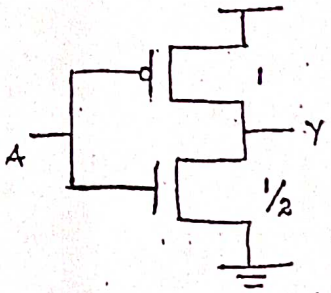
* If one input transition is more important than the others, the skewed gates are used.
* HI skew gates are used to favour the rising output transition.
* Lo skew gates are used to favour the falling output transition.
* This can be done by decreasing the size of noncritical transistor.
* Logical effort for falling transition = g_d

  Logical effort for rising transition = g_u

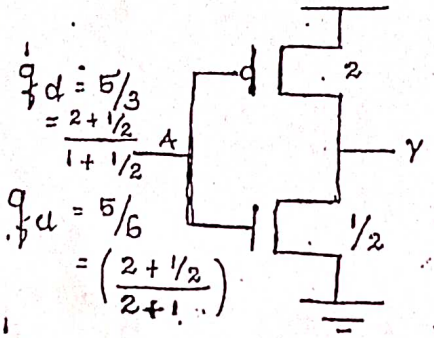
$$g_d \text{ (or) } g_u = \frac{\text{i/p capacitance of skewed gate}}{\text{i/p capacitance of unskewed inverter}}$$



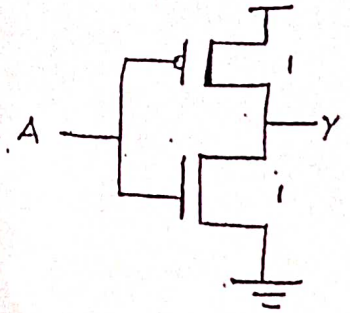
unskewed inverter
(equal rise resistance)



unskewed inverter
(equal fall resistance).



HI skew inverter



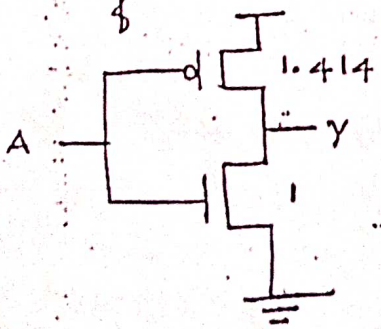
$g_d = 2/3$

$g_u = 4/3$

LO skew inverter.

P/N Ratio:

* Reducing the PMOS size from 2 to $\sqrt{2} = 1.414$ for the inverter gives the fastest average delay. But this delay improvement is only 2%.
* This reduces the PMOS area, capacitance, power consumption, and this moves the switch point lower and reduces the noise margin.



$g_u = 1.15$

$g_d = 0.81$

Multiple threshold voltages:

* Some CMOS process offers two or more threshold voltages. Transistor with lower threshold voltage produces more ON current, but leaks more OFF current exponentially.

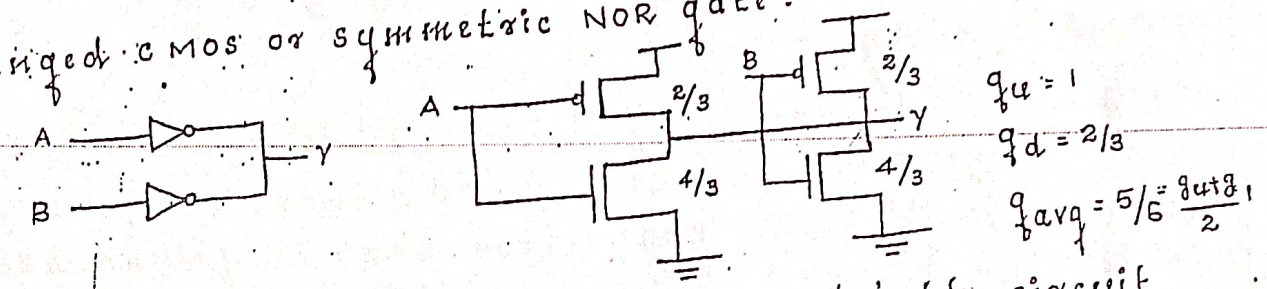
) Ratioed circuits :-

a) Ganged EMOS

b) Source follower pullup

c) pseudo NMOS

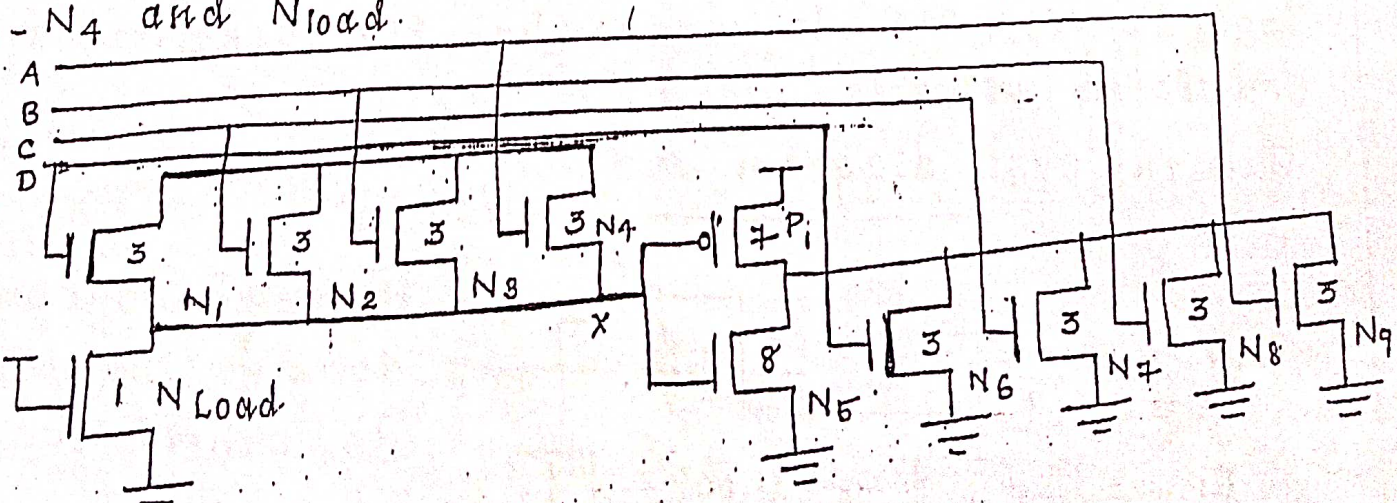
a. Ganged CMOS or symmetric NOR gate :



* When one input is '1', and the other is '0', the circuit operate as a pseudo NMOS.
* When both inputs are '0', both PMOS turns ON in parallel, pulling the o/p faster than in pseudo NMOS.
* When both inputs are 1, both PMOS are off, reducing static power dissipation.

b) Source follower pullup Logic : (SFPL)

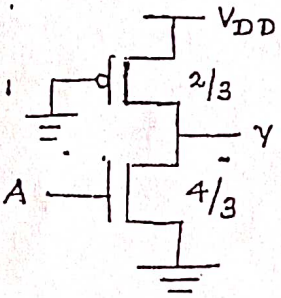
* 4 input NOR gate.
* pullup is controlled by input.
* N_6 - N_9 and P_1 form pseudo NMOS NOR.
* Gate of pullup 'P_1' is controlled by source follower N_1 - N_4 and N_{load}.



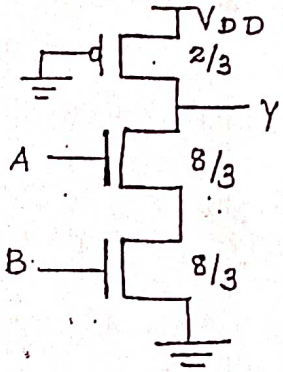
* When one input turns ON source follower pulls node x to approximately $V_{DD}/2$.
* This partially turns off P_1. which allows smaller nMOS pulls downs N_6-N_9 to be used.
* SEPL is used for constructing wide NOR gates.

c) Pseudo n-MOS :-

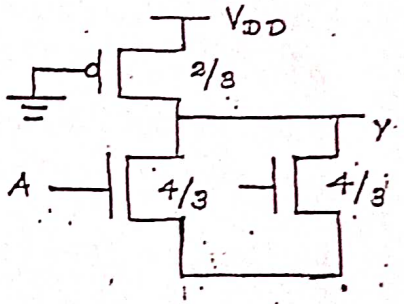
* In Pseudo nMOS, the pull down network is like that of a static gate, but the pull up network is replaced with a single PMOS transistor that is grounded so it is always ON.
* Pseudo nMOS is useful for fast wide NOR gates or NOR based structures like (ROM and PLA)



Inverter



NAND gate

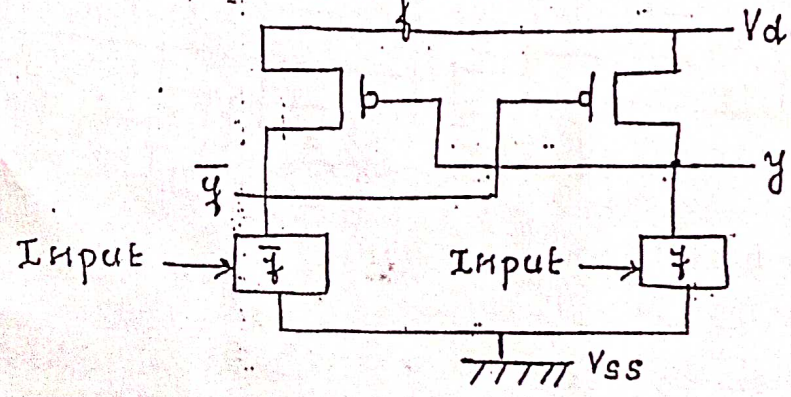


NOR gate

(+) Cascade voltage switch Logic :

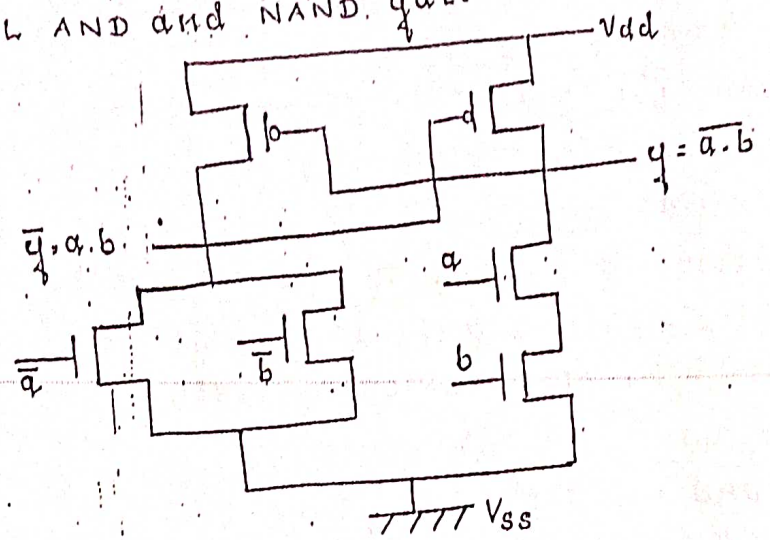
* It is also known as differential cascade voltage switch logic (DCVSL). Cascade means that the transistors are connected in series.

General CVSL diagram



for any i/p, one pull down network is ON and other is OFF.

VSL AND and NAND gate



Advantages:

① Its speed is good, because all logic performed with N-MOS. So input capacitance is reduced.

⑧ Dynamic circuits:

Advantages

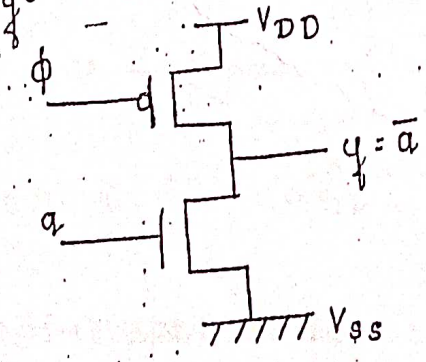
i) It has lower input capacitance

ii) No contention during switching.

iii) It has zero static power dissipation

Operating modes:—

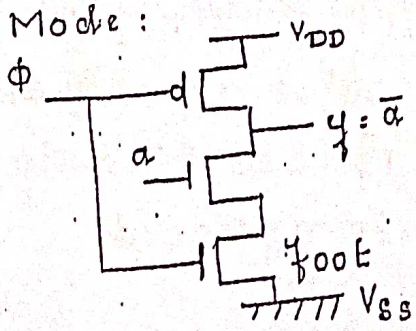
i) Precharge Mode:

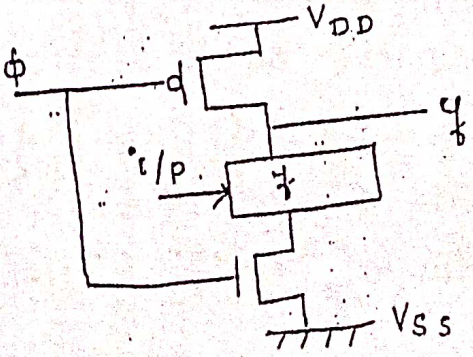


* Here, ϕ is '0'

So clocked PMOS is ON. y = 1

ii) Evaluate Mode:





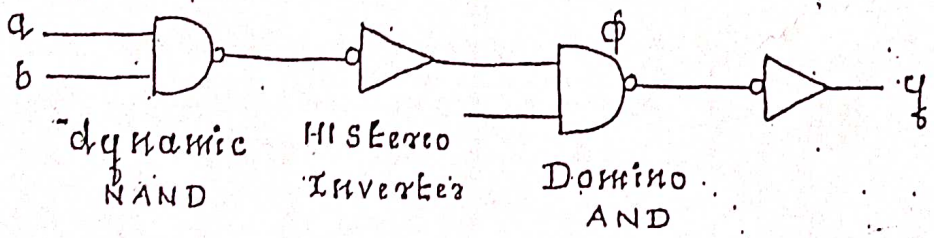
* Here clock ϕ is '1', clocked pMOS is OFF, The o/p may remain high or discharged low.
* If the input cannot be '0' during precharge, an extra transistor can be added at the bottom of the nMOS stack. It is known as foot.
* Monotonicity requirement is one of the difficulty in the dynamic circuits. While a gate is in evaluation mode, the inputs must be monotonically rising.

It means, the input can,

→ start Low and remain Low (00)
→ start Low and rise High (01)
→ start High and remain High (11)

a) Domino Logic :-

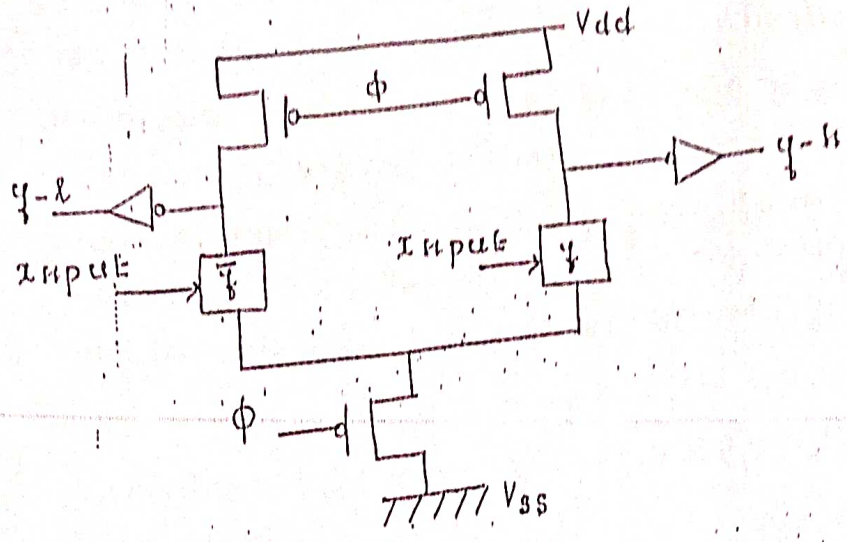
* The monotonicity problem can be solved by connecting a static CMOS inverter between the dynamic gate.
* It is used to convert monotonically falling output into a monotonically rising signal suitable for the next gate.
* The dynamic static pair is known as domino gate
* HI skew gate is used as static inverter.



b) Dual-Rail Domino Logic :-

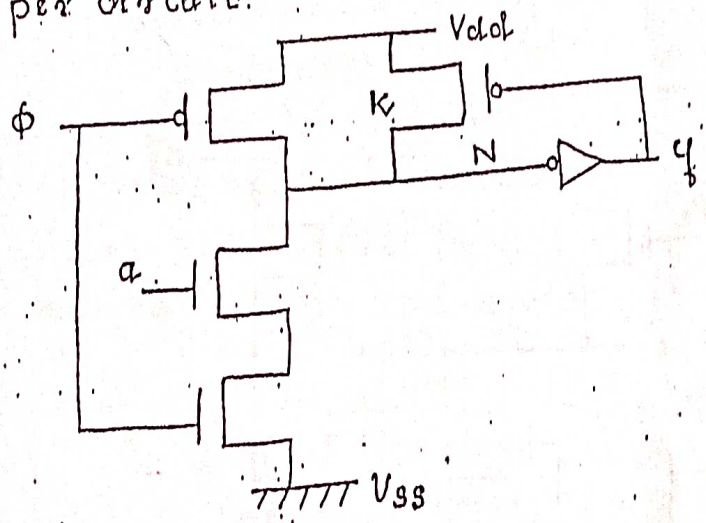
* It is a dynamic form of cascade voltage switch logic.
* It encodes each signal with a pair of wires. The input and output signal pairs are -h and -l.

→ If the o/p is '1' then -h is asserted.
→ If the o/p is '0' then -l is asserted.



→ Keeper Implementation :-

* Leakage and Noise margin problems are addressed by keeper circuit.



* If dynamic node N is high, y is low and keeper circuit is ON to prevent N from floating.
* If N falls, the keeper circuit initially opposes the transition. so it must be much weaker than the pull down network.
* The keeper must be wide to compensate for any leakage current drawn when the o/p is floating and pulldown network is OFF.
* Noise margin can be improved by using strong keepers.

c) Multiple output domino Logic :- (MODL)

* If one function is a subfunction of another subfunction, then, multiple output domino Logic is needed.
* It saves area by combining all the functions into a multiple output gate.
* Main application of MODL is an addition operation.

$$C_1 = g_1 + P_1 C_0 \quad -(i)$$

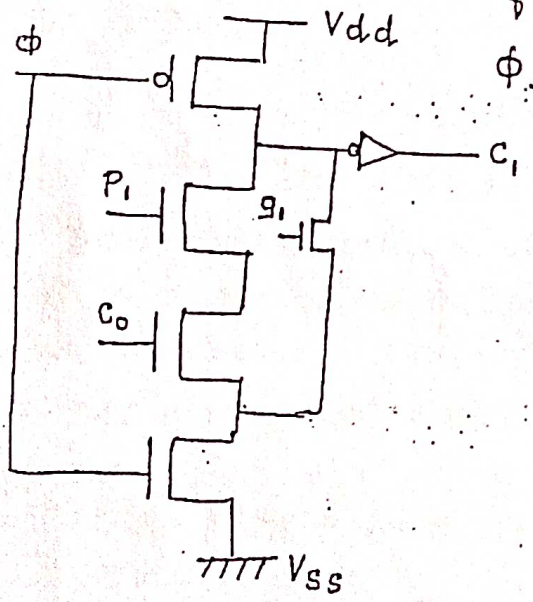
$$C_2 = g_2 + P_2 (g_1 + P_1 C_0) \quad -(ii)$$

$$C_3 = g_3 + P_3 (g_2 + P_2 (g_1 + P_1 C_0)) \quad -(iii)$$

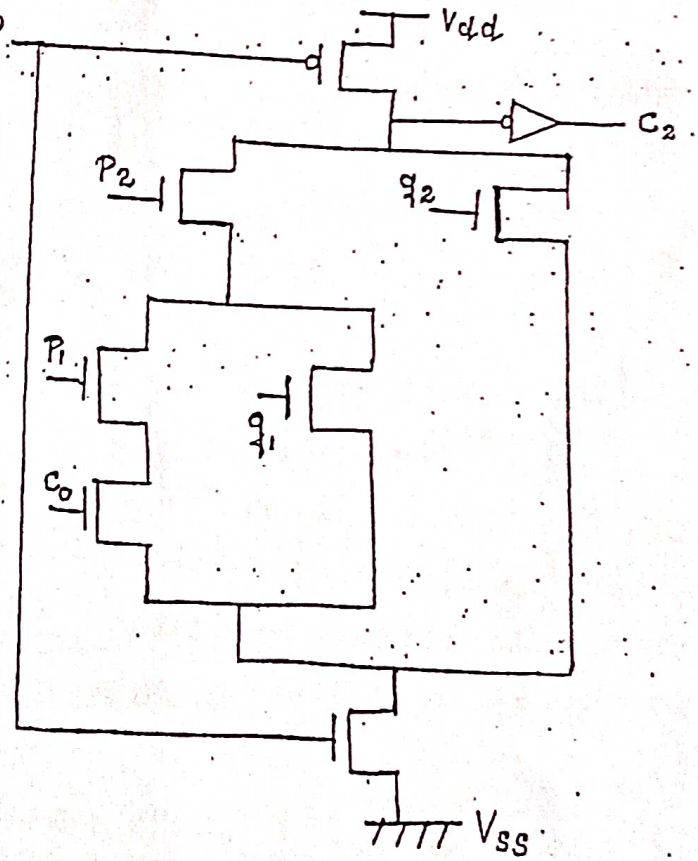
} → Manchester Carry chain

Where, C_i → Carry , g_i → generate

P_i → propagate , i → bit position in the block



$C_1 = g_1 + P_1 C_0$

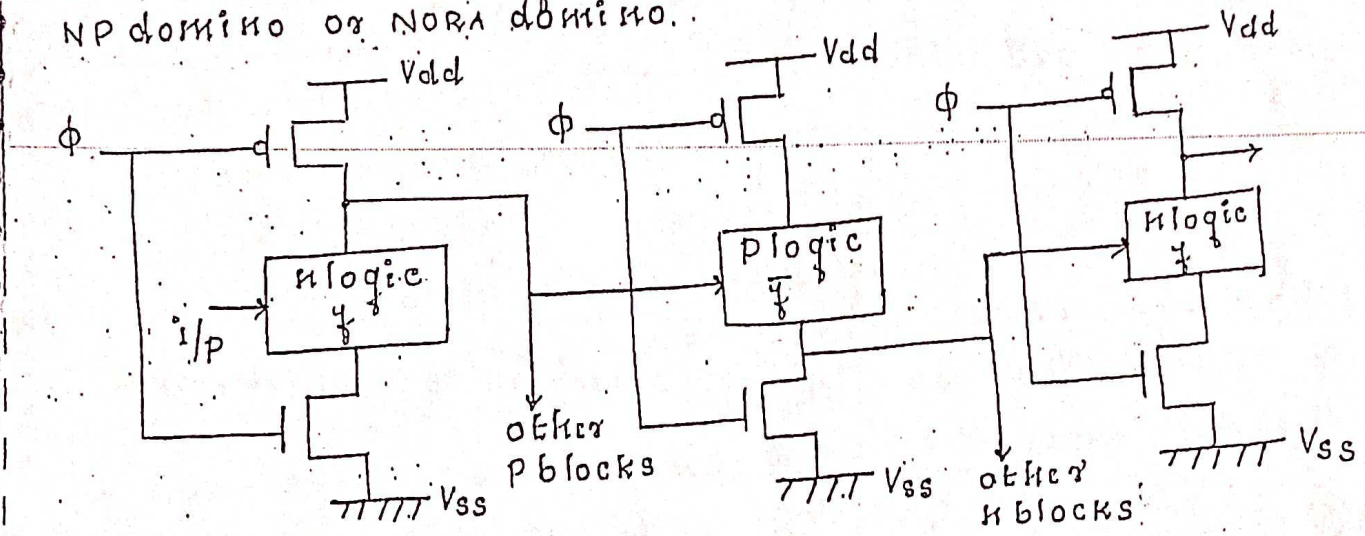


$C_2 = g_2 + P_2 (g_1 + P_1 C_0)$

d) NP Domino :-

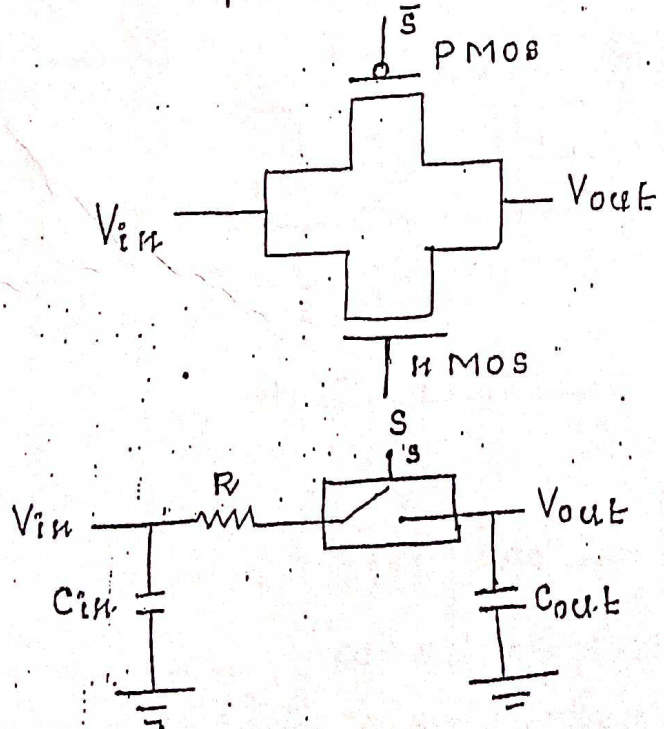
When ϕ is Low first and third stages precharge high, second precharges Low.

When ϕ rises, all stages evaluate. This style is called NP domino or NORA domino.



e) Pass transistor circuits :-

* Transmission gate is nothing but the parallely connected p-MOS and n-MOS.



Switching model

$R \rightarrow \max(R_n, R_p)$

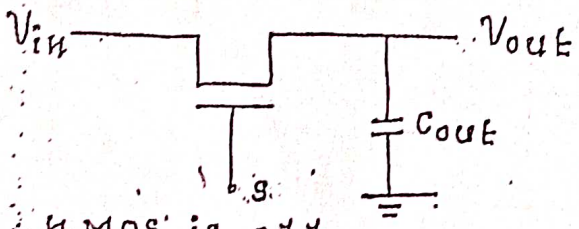
$R_n \rightarrow$ (n refers nMOS) nMOS Resistance

$R_p \rightarrow$ (p refers p-MOS) pMOS Resistance

* The transmission gate acts as voltage controlled resistor connecting the input and output.
* It can be used as a logic structure, switch, latch element etc.

Operation of transmission gate:

i) nMOS pass transistor:-



→ When $S=0$, nMOS is off

→ When $S=1$, $V_{in} = V_{DD}$, initial condition of V_{out} (at $t=0$) $= 0$

→ $V_{out}(t) = V_{max} \cdot \frac{t/2\,\tau_n}{1 + t/2\,\tau_n}$

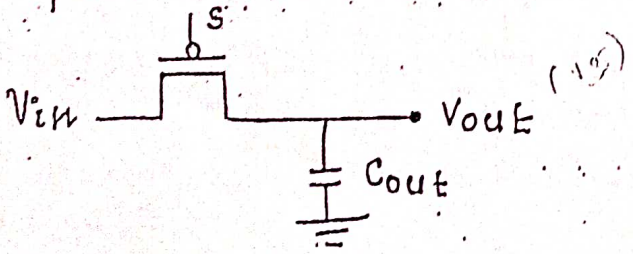
→ $V_{max} = V_{DD} - V_{tn}$ ⇒ maximum voltage that can be transfered through nMOS.

→ When limit $t \to \infty$, then

$$\lim_{t \to \infty} V_{out}(t) = V_{max}$$

→ t_r = Rise time = $18\,\tau_n = 18\,R_n C_{out}$

ii) PMOS pass transistor :-



$\tau_p = R_p \cdot C_{out}$

→ When $\bar{S} = 1$ ($S = 0$), $V_{in} = V_{DD} \Rightarrow V_{out} = V_{SS}$

→ When $\bar{S} = 0$ ($S = 1$), $V_{in} = V_{SS} \Rightarrow V_{out} = V_{DD}$

At this stage t discharges through pmos until $V_{out} = V_{tp}$. (At this point transistor stops conducting)

$t_f = 2.94 \tau_p$, $\tau_p = R_p \cdot C_{out}$

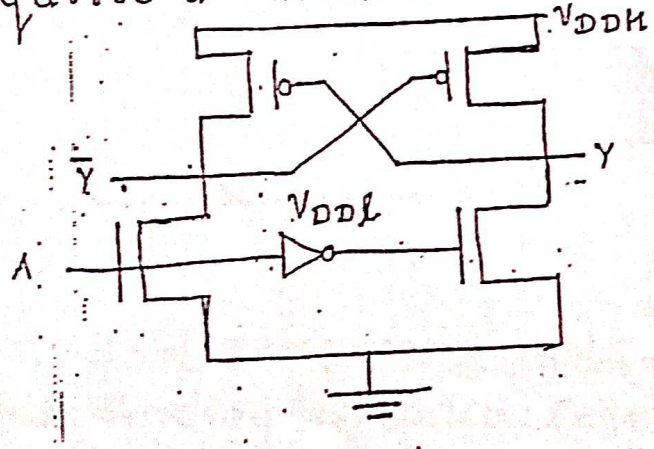
LOW POWER LOGIC DESIGN

* Various techniques used to achieve low power dissipation

i) Dynamic power reduction

ii) To adjust the power supply is to divide the logic into
   a) high speed supply
   b) low speed supply

* Fast logic is connected to high supply
* Slow logic is connected to low supply
* Level converter has to be inserted between two styles of logic.
* Interface between high V_{DD} to low V_{DD} is a direct connection, Interface between low V_{DD} to high V_{DD} requires a Level converter.



iii) The activity factor plays an important role in power savings.

CMOS Logic → 0.1

Dynamic Logic → 0.5

Clocks → 1

If i/p do not switch → 0

* In unused units, if the clock is gated to register, then the power is saved.

iv) Minimum sized, complementary CMOS with a P/N ratio is the best for low power option.

COMPARISON OF CIRCUIT FAMILIES

* Static CMOS Logic is best for CMOS circuits. It is fast.
* Pseudo nMOS, dynamic NOR gates are suitable for implementing high fan-in functions. Because logical effort is independent of the width.

E.g: PLA, ROM

* Domino Logic is suitable for high speed applications.

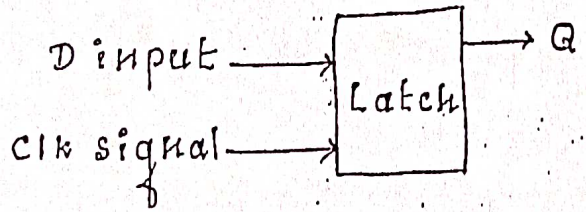
SEQUENCING STATIC CIRCUITS

① Elements used in sequential circuits

a) Latches

b) flip-flops.

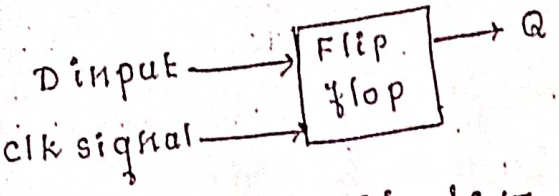
a) Latches :-



* If clock is high, D input flows through to Q. If clock is low, then the Latch holds its present Q value even if D changes.

b) Flip flop :-

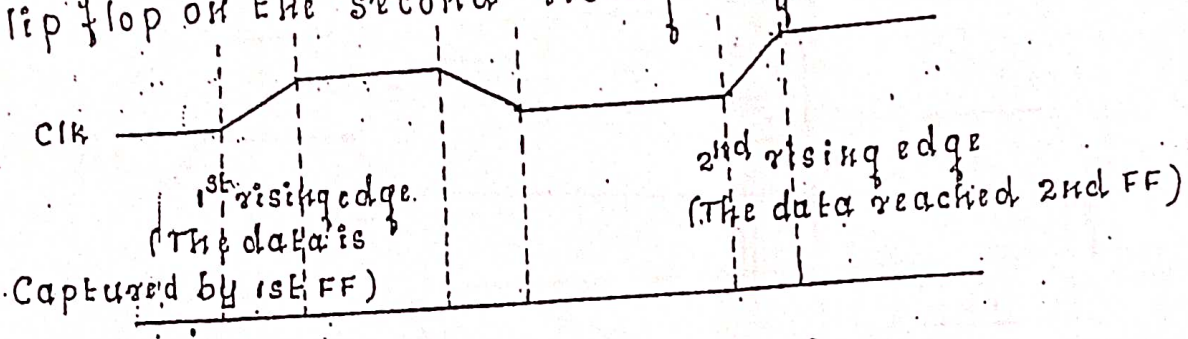
* It is an edge triggered device, during the rising edge of the clock, Q value is nothing but D value. D value is ignored at all other times.



② Sequencing Methods :-

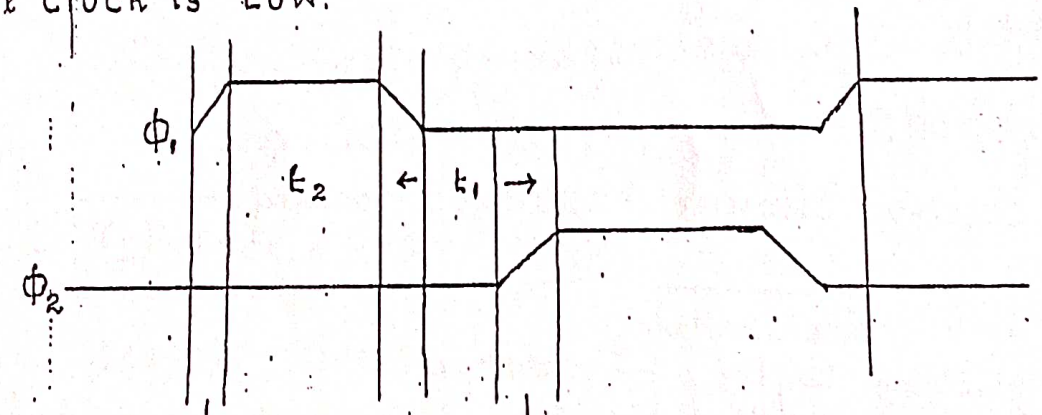
→ Method 1 : (Flip flop system)

* The data is captured in the first flop during the first rising edge of the clock. It is propagated through the combinational logic block and it reaches the second flip flop on the second rising edge of the clock signal.



→ Method 2 : (2 phase Latches System)

* Here 2 clocks ϕ_1 and $\bar{\phi}_2$ are used. At any time, atleast one clock is Low.



data latched during rising edge of ϕ_1

data reaches 2nd latch during rising edge of ϕ_2

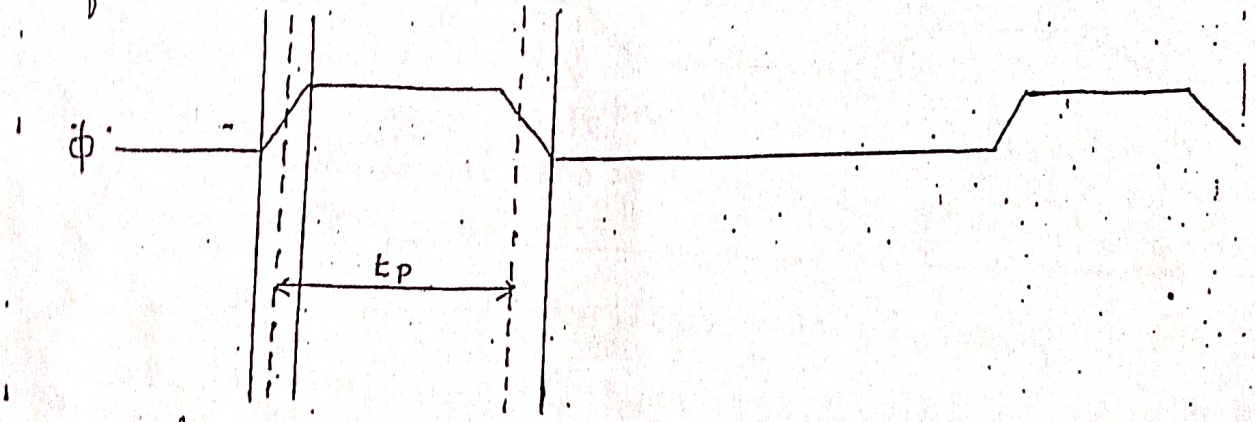
* The phases are separated by t_1.

* The data is latched into 1st Latch during the rising edge of ϕ_1. The data is processed by combinational Logic block. Then it reaches 2nd Logic during the rising edge of ϕ_2.

* Then the data is processed by combinational Logic block.

→ Method 3: (Pulsed Latch system)

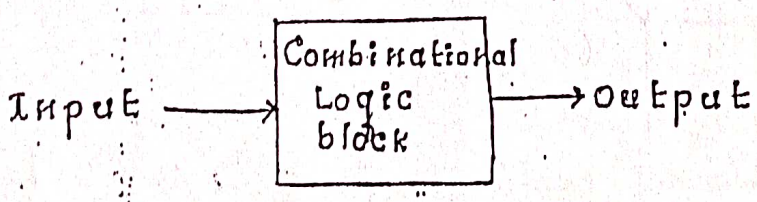
* Here one latch is eliminated from each cycle.
* If the pulse is shorter than the delay through the combinational logic block, then the data can be expected further.
* The data is Latched by Latch during the rising edge of ϕ. Then it is propagated through the combinational Logic block.



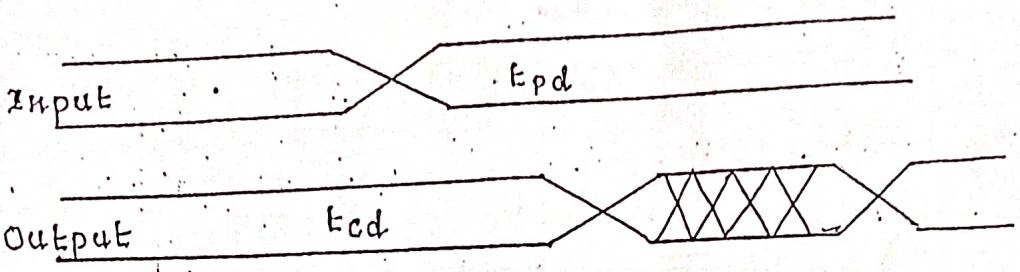
data is latched into latch tp = pulse width

③ Timing diagram :-

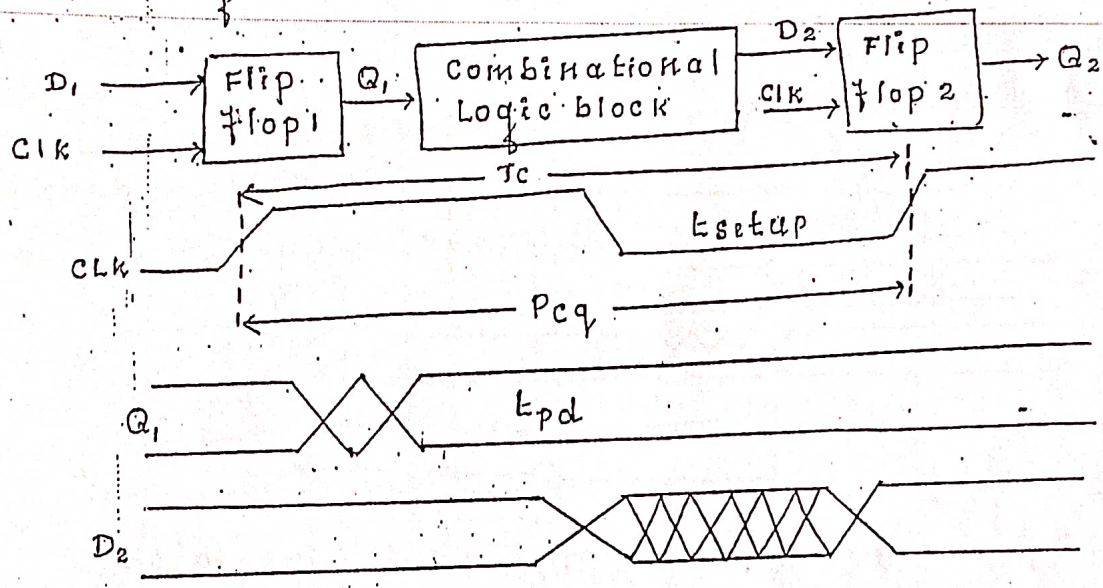
* The output cannot change instantaneously.



* After some delay the output start to change. This delay is known as contamination delay. (t_{cd})
* After some delay, the output is settled to a final value. This delay is known as propagation delay (t_{pd})



(4) Max-delay constraints :-



t_{pd} → Logic propagation delay

t_{pcq} → Latch/flipflop clock to Q propagation delay

→ $\boxed{T_c \geq t_{pcq} + t_{pd} + t_{setup}}$

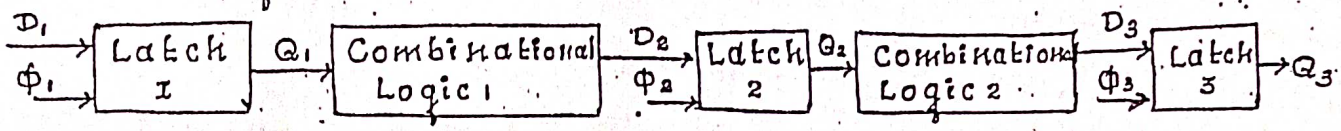
* If a combinational logic delay is too high, then the receiving element can miss its setup time. So it samples the wrong value. It is known as setup time failure (or) Max-delay failure.

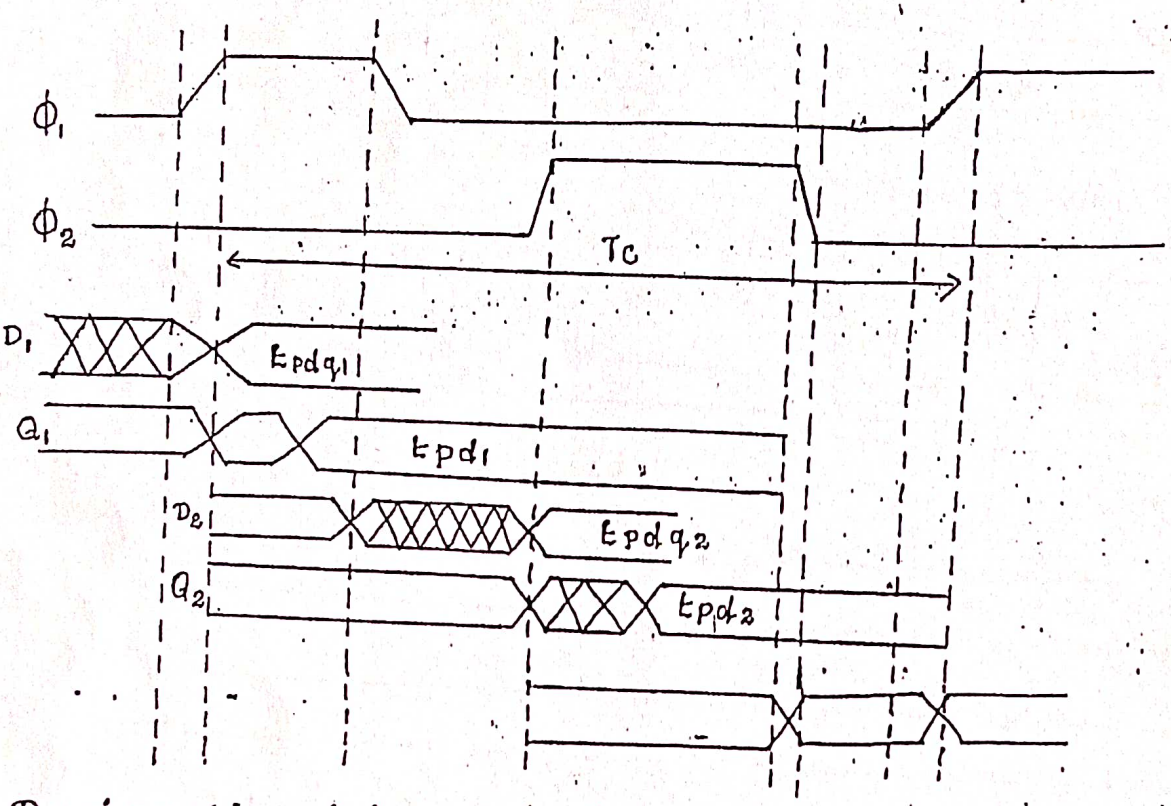
* To overcome this failure, the logic can be redesigned or the clock period can be increased.

$$t_{pcq} + t_{pd} + t_{setup} \leq T_c$$

* Maximum allowable logic delay can be $t_{pd} \leq T_c - (t_{setup} + t_{pcq})$

a) Max. delay constraint of 2 phase latch :-





* During the rising edge of ϕ_1, D_1 is latched in to latch 1. Then it is propagated through combinational Logic 1 block then through latch 2, then through combinational Logic 2 block.

→ Time borrowing :-

* Certain paths longer time if other paths take less time. This technique is known as time borrowing.

$$T_c \geq t_{pdq_1} + t_{pd1} + t_{pdq_2} + t_{pd2}$$

$$t_{pd} = t_{pd1} + t_{pd2}$$

$$T_c \geq t_{pd} + t_{pdq_1} + t_{pdq_2}$$

$$t_{pd} \leq T_c - (t_{pdq_1} + t_{pdq_2})$$

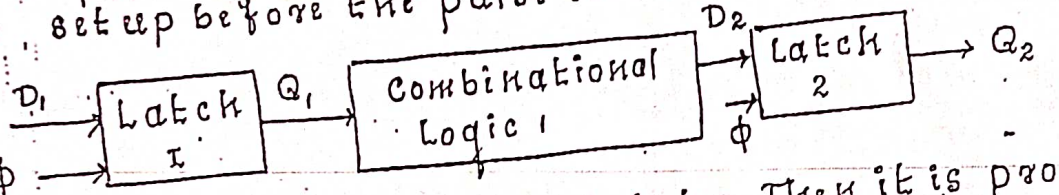
Where, t_{pd} → Logic propagation delay

t_{pdq} = Latch D to Q propagation delay

Max. delay constraint of Pulsed Latch system:-

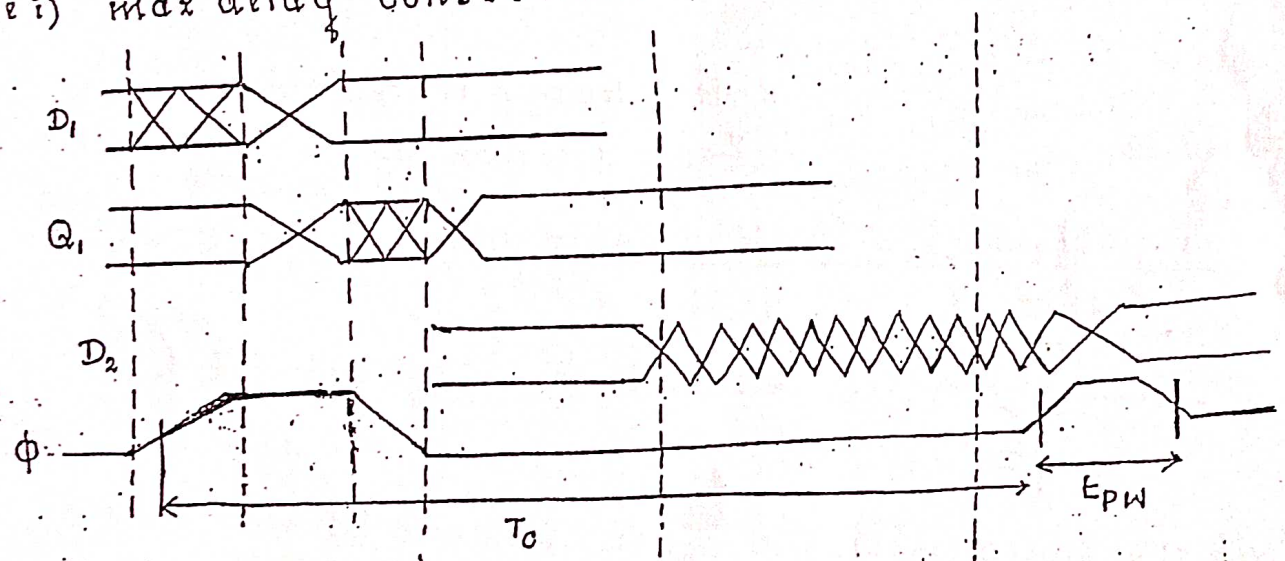
If the pulse is wide enough then, the max delay constraint is similar to 2 phase latch system.

If the pulse is narrower than the setup time, the data must setup before the pulse rises.

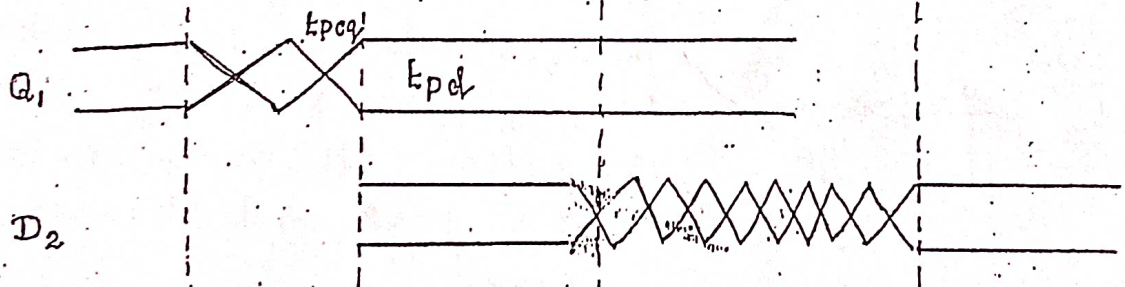


* The data D_1 is latched into Latch 1. Then it is propagated through combinational Logic block and then it is propagated through Latch 2.

Case i) max delay constraint, if $t_{pw} > t_{setup}$



Case ii) if $t_{pw} < t_{setup}$



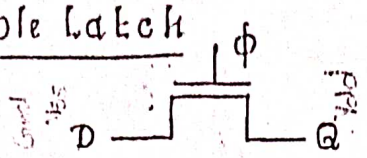
$\rightarrow T_c \geq \max(t_{pdq} + t_{pd},\ t_{pcq} + t_{pd} + t_{setup} - t_{pw})$

$$t_{pd} \leq T_c - \max(t_{pdq},\ t_{pcq} + t_{setup} - t_{pw})$$

CIRCUIT DESIGN OF LATCHES AND FLIPFLOPS

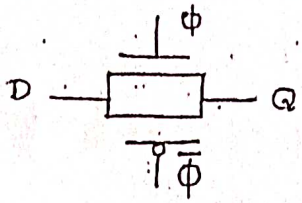
i) Conventional CMOS Latches :-

a) simple Latch



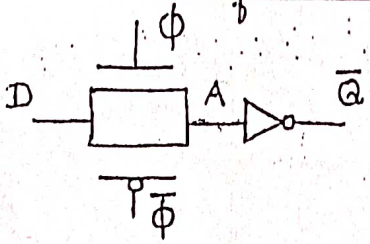
* The o/p doesnot swing from Gnd to V_{DD}.

b) CMOS transmission gate instead of NMOS



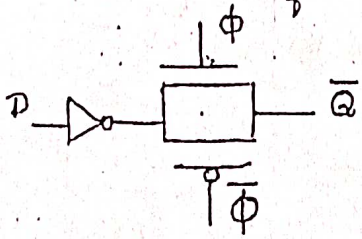
* It needs $\bar{\phi}$ clock also.

c) Transmission gate with output inverter



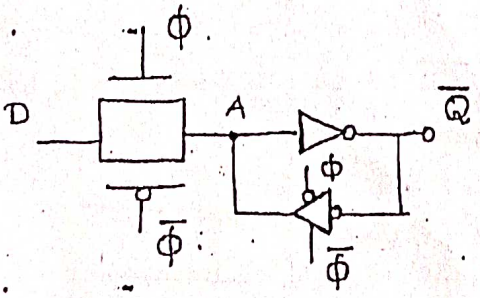
* Here node A is isolated from noise on o/p.

d) Transmission gate with inverter added at the input

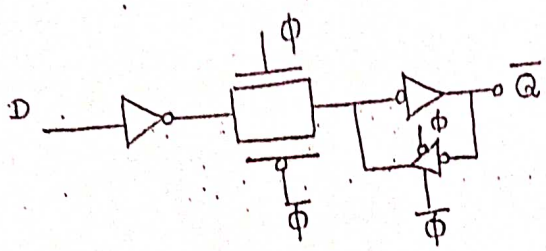


* This is fast dynamic latch

e) Feedback added with the fast dynamic Latch :

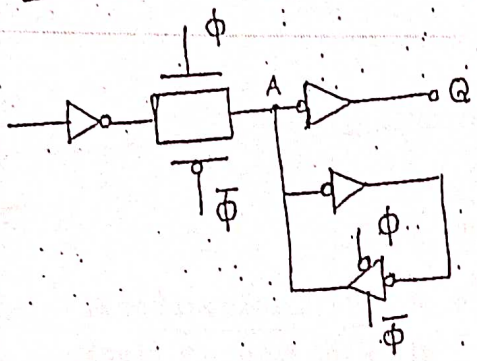


* Feedback is added to prevent the o/p from floating. The noise in the o/p can be given to state node through feedback.

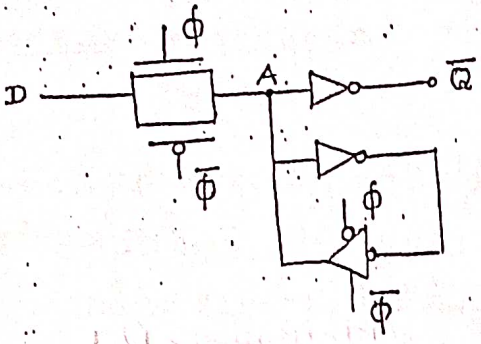


* Inverter is added in the input.
* The noise in the o/p can be given to state node through feedback.

b) Latch which overcome all the above said problems

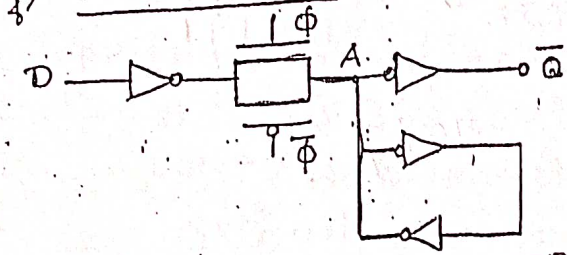


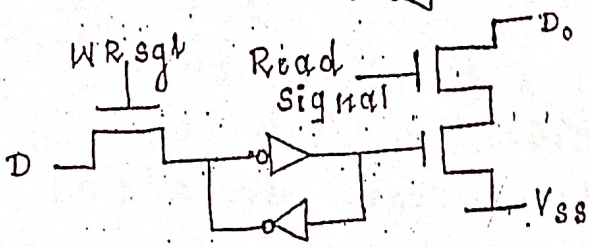
* It is used in standard cell applications.
* This is static and all nodes swing Gnd to Vdd. State noise is isolated from o/p noise.



* It is faster and used by INTEL.
* It is suitable for semicustom datapath applications.

g) Jamb Latch

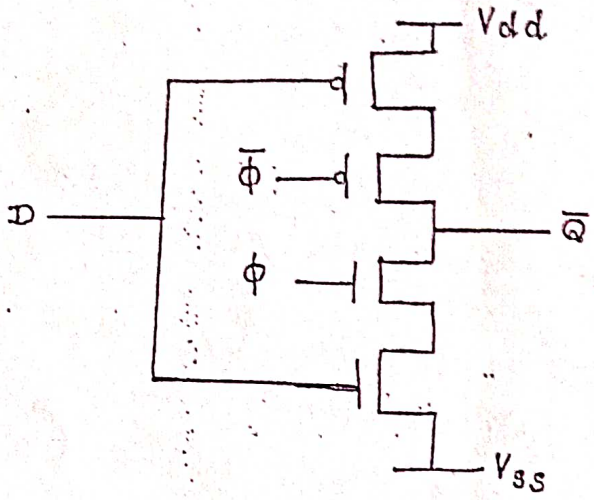




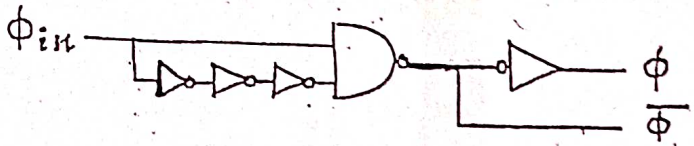
* It is similar to (f). But here tristate is replaced by inverter. Φ and Φ̄ clock signals are avoided here. It is known as Jamb Latch.

* It is used in FPGA Cells.

h) C^2MOS Latch

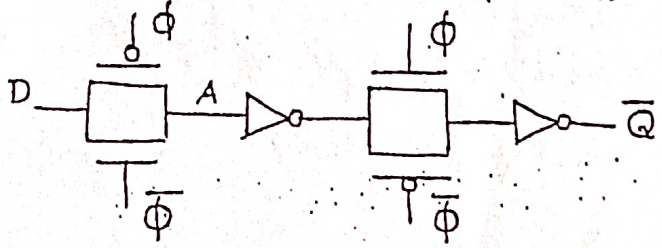


PULSED LATCHES :-



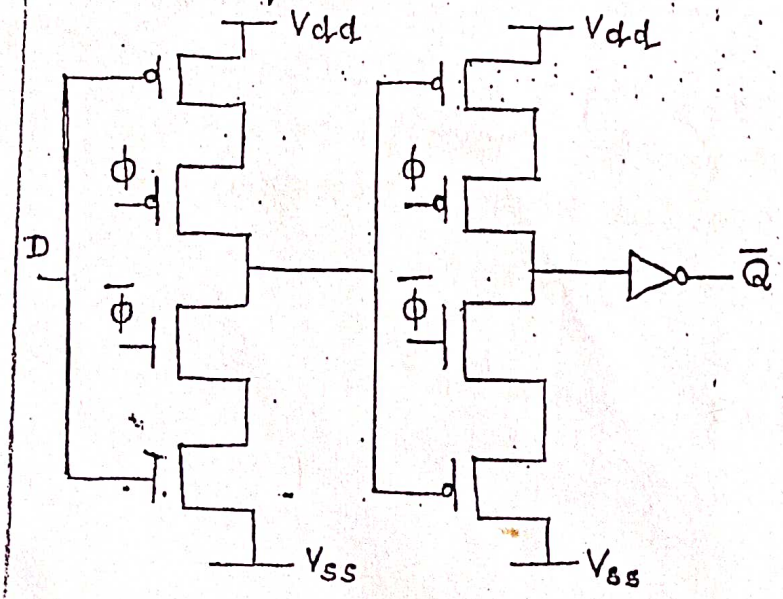
* Pulse generator is also known as clock chopper or one-shot.

Conventional CMOS Flip flop :-



* It is formed by connecting two dynamic latches back to back.

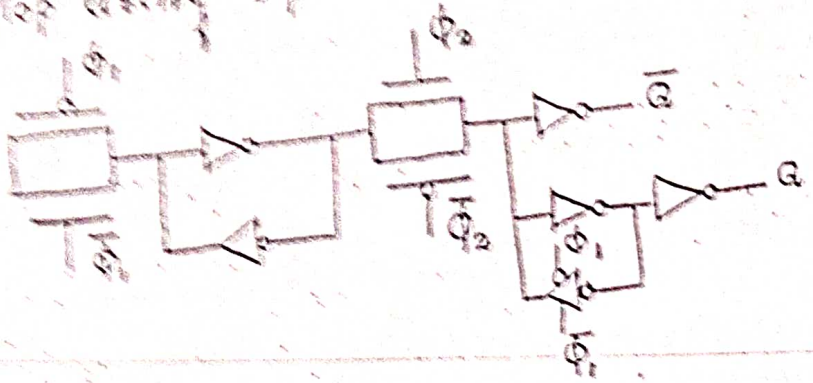
① NORA dynamic flip-flop :-



* It is formed by using C^2MOS Latches. It is also known as C^2MOS dynamic flip flop.

* The problem in this circuit is that both transistors partially ON due to very slow edge rates.

Flipflop using 2 phase non overlapping clocks



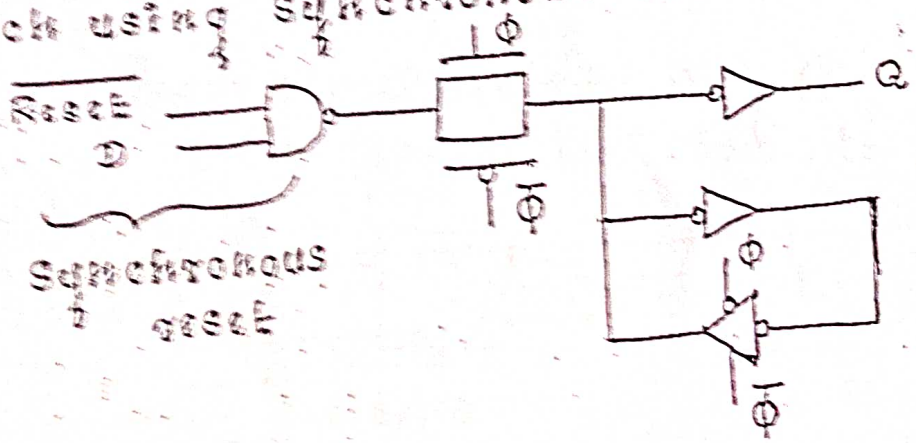
* To avoid minimum delay problems
* Here ϕ_1, ϕ_2 are 2 phase non overlapping clocks.

Resettable Latches and Flipflops

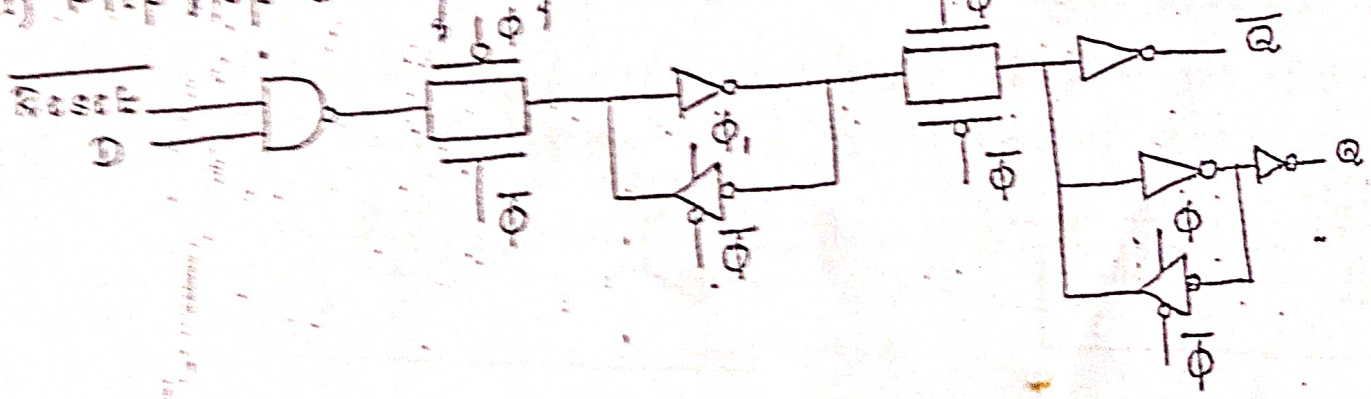
Reset

- Synchronous reset (It must be stable for a setup and hold time around the clock edge).
- Asynchronous reset (It forces Q low immediately)

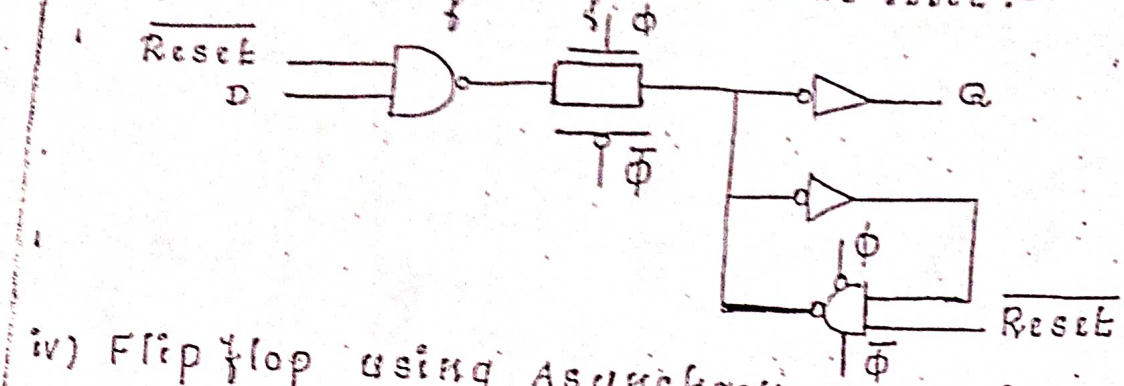
i) Latch using Synchronous reset :-



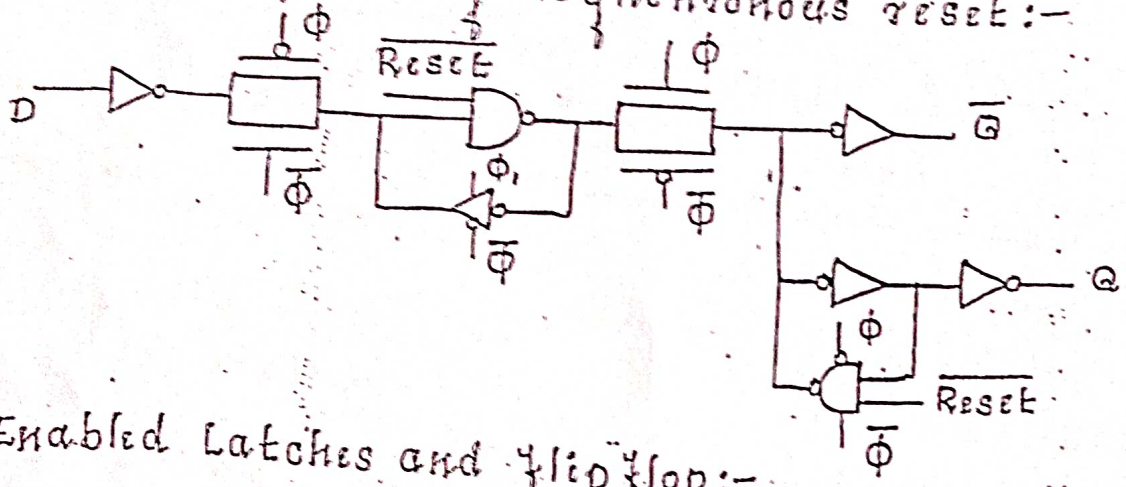
ii) Flipflop using synchronous reset :-



iii) Latch using Asynchronous reset :-

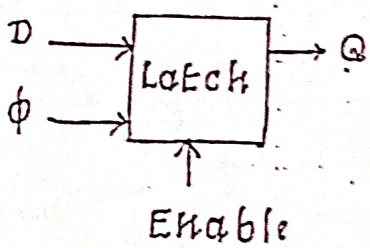


iv) Flip flop using Asynchronous reset :-

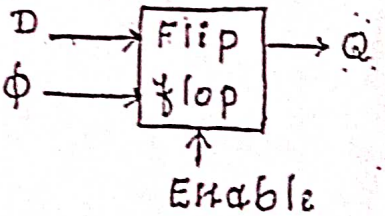


Enabled Latches and flip flop :-

* Enable signal is introduced in enabled Latches and Flip flops.
* If enable is low, the element retain its state independently of the clock.

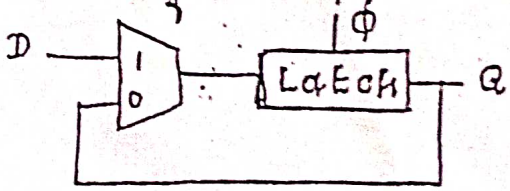


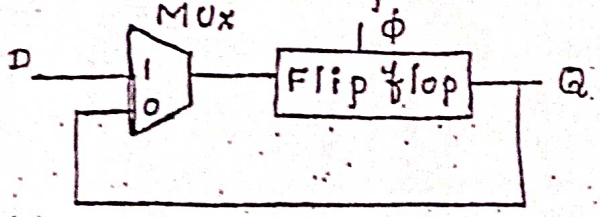
Enable Latch symbol



Enable flip flop symbol.

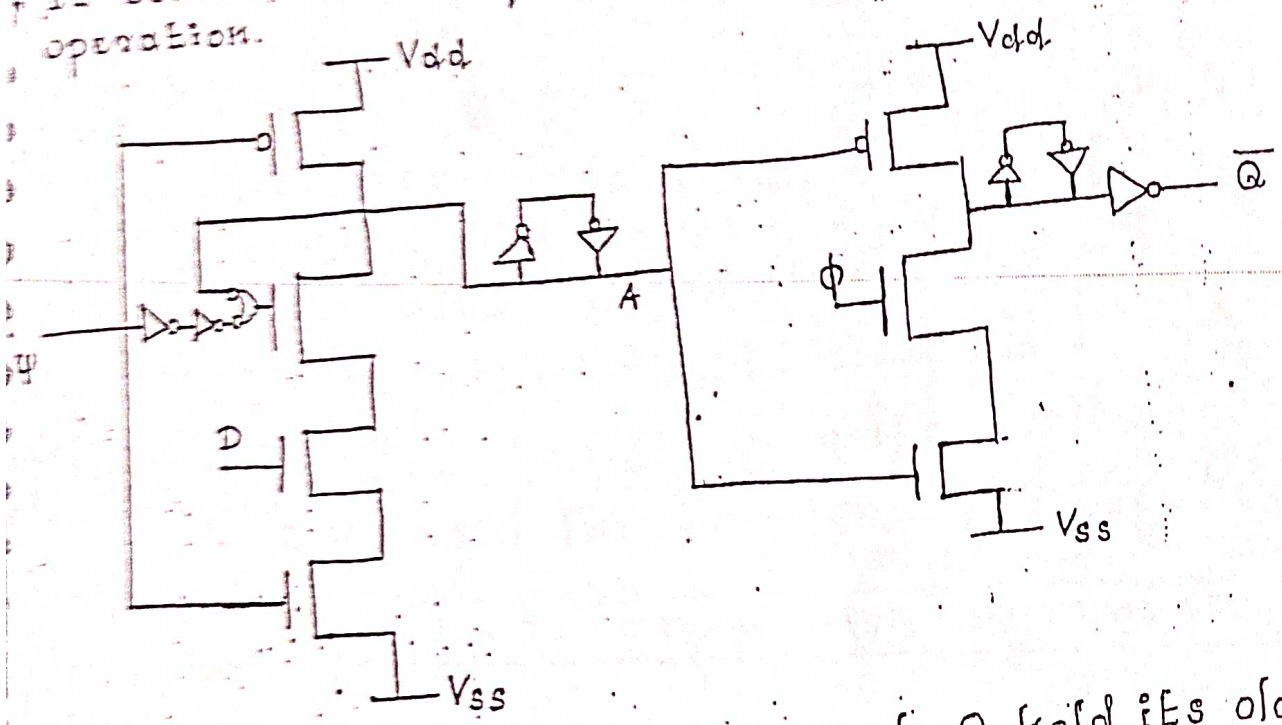
* When the element is disabled, then the old state is feeding back to the i/p of the multiplexer.





Class Semidynamic flipflop :-

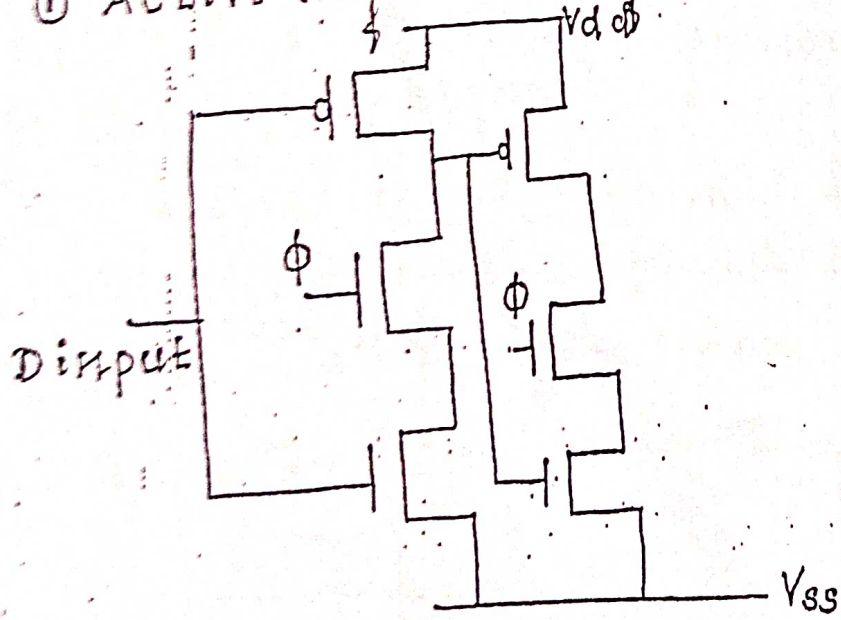
* It combines the dynamic input stage with static operation.



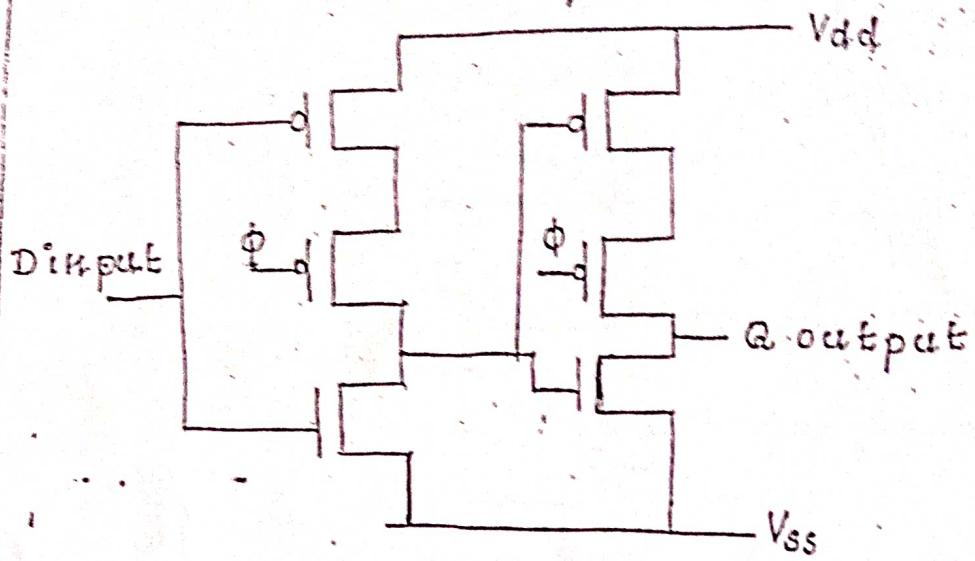
* If Φ is Low, A prechanges high. Q hold its old stage
* When Φ rises, the dynamic NAND evaluates.
* If D is '0', A remains high and top nMOS is off.
  If D is '1', A starts to become low. then nMOS is ON.

True single phase clock Latches and flipflops (TSPC) :-

① Active high TSPC dynamic Latch



ii) Active Low TSPC dynamic Latch:-



iii) TSPC dynamic flip flop :-

* Combined form of Active low and high Latches.

STATIC SEQUENCING ELEMENT METHODOLOGY

→ Choice of elements

① Flip flop
- * It has high sequencing over head
- * simple
- * Good choice for CAD tools.

② Pulsed Latches
- * faster
- * offer time borrowing capability
- * high hold time
- * Low power consumption
- * Easily integrated
- * Long hold time - makes the pulsed Latches unsuitable.

) Transparent Latches :-

* Lower sequencing overhead
* Data can arrive at the Latch anytime the Latch is transparent.

> Low power sequential design:

* Flipflop and Latches are clocked every cycle. clock gating can be used for reducing the power.
* Pulsed Latches are more efficient.

→ Two phase timing Latch

* In this type, the signal can belongs to phase 1 or phase 2. In each phase, 3 different clocks are there. These are stable, valid, qualified clock.

a) stable clock:

* A signal is stable (in ϕ_1) if it settles to a value before ϕ_1 rises and remains const until after ϕ_1 falls.

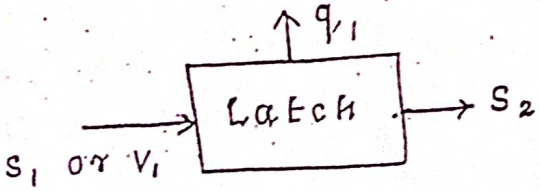
b) Valid clock:

* A signal is valid (in ϕ_1) if it settles to a value before ϕ_1 falls and remains at the value until after ϕ_1 falls.

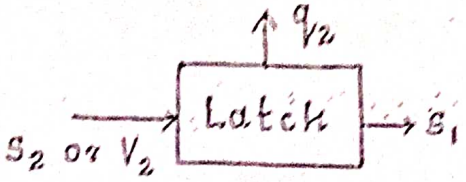
c) Qualified signal:

* A signal is said to be in qualified clock in ϕ_1, if it either rises and falls like ϕ_1 or remains low for the entire cycle.

→ Rules for combining Timing Types

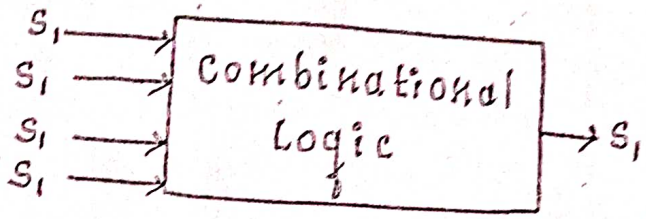


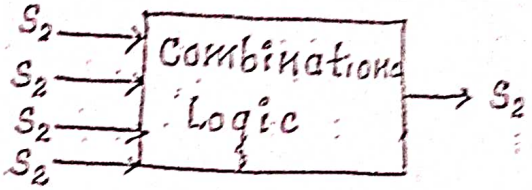
q_1 → qualified signal
S_1 → Stable signal
S_2 → stable signal
V_1 → Valid signal



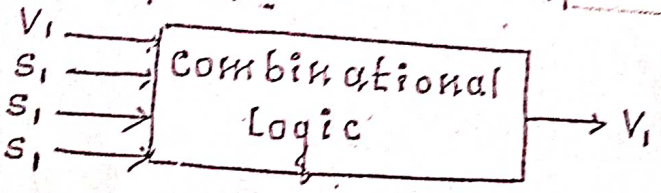
S_2 - stable signal in ϕ_2
S_1 - stable signal in ϕ_1
V_1 - Valid signal in ϕ_2
q_2 - qualified clock in ϕ_2

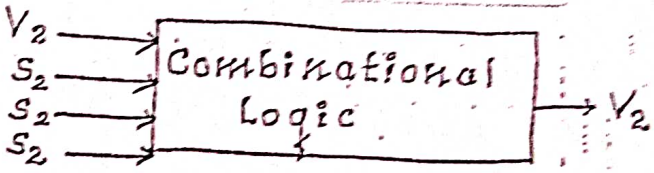
* If the inputs are stable, then the o/p is stable.



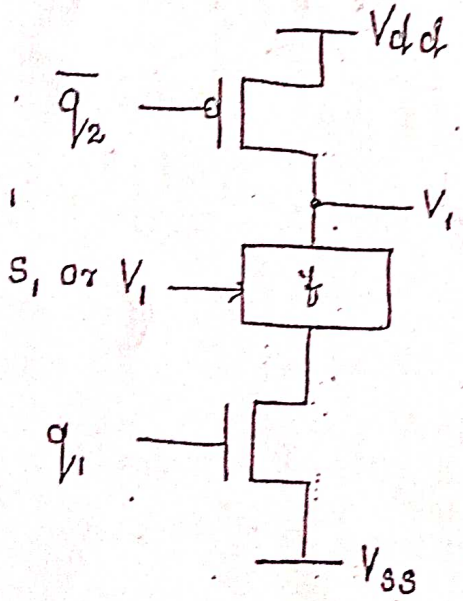


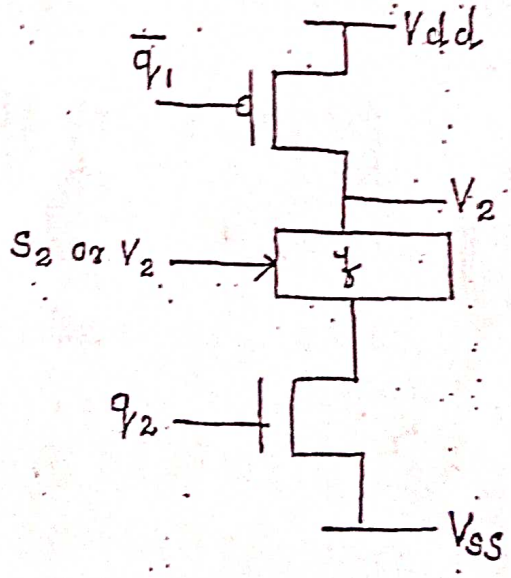
* If any one of the i/p is valid, then the o/p is valid.





* If input is S_1 (or) V_1, then the o/p is V_1.





Characterizing Sequencing Element delays :-

* The delay is varied with input slope, voltage and temperature.
* If delay is added on the clock, t_{pcq} is chosen to minimize the sequencing overhead $t_{setup} + t_{pcq}$
* If t_{buf} is added,

$t_{setup1} = t_{setup} + t_{buf}$

$t_{pcq1} = t_{pcq}$

$t_{hold1} = t_{hold} - t_{buf}$

SEQUENCING DYNAMIC CIRCUITS

* Precharge mode and evaluation mode are two operating modes of dynamic and domino circuits.
* The delay of a path is the sum of the evaluation delays of each gate along the path.
* The input of dynamic gate is monotonically rising during evaluation mode. It produces monotonically falling outputs

④ Traditional Domino Circuits :-

* If the clock is high, the first half cycle evaluates and second half cycle precharges.
* If the clock is low, the second half cycle evaluates and the first half cycle precharges.

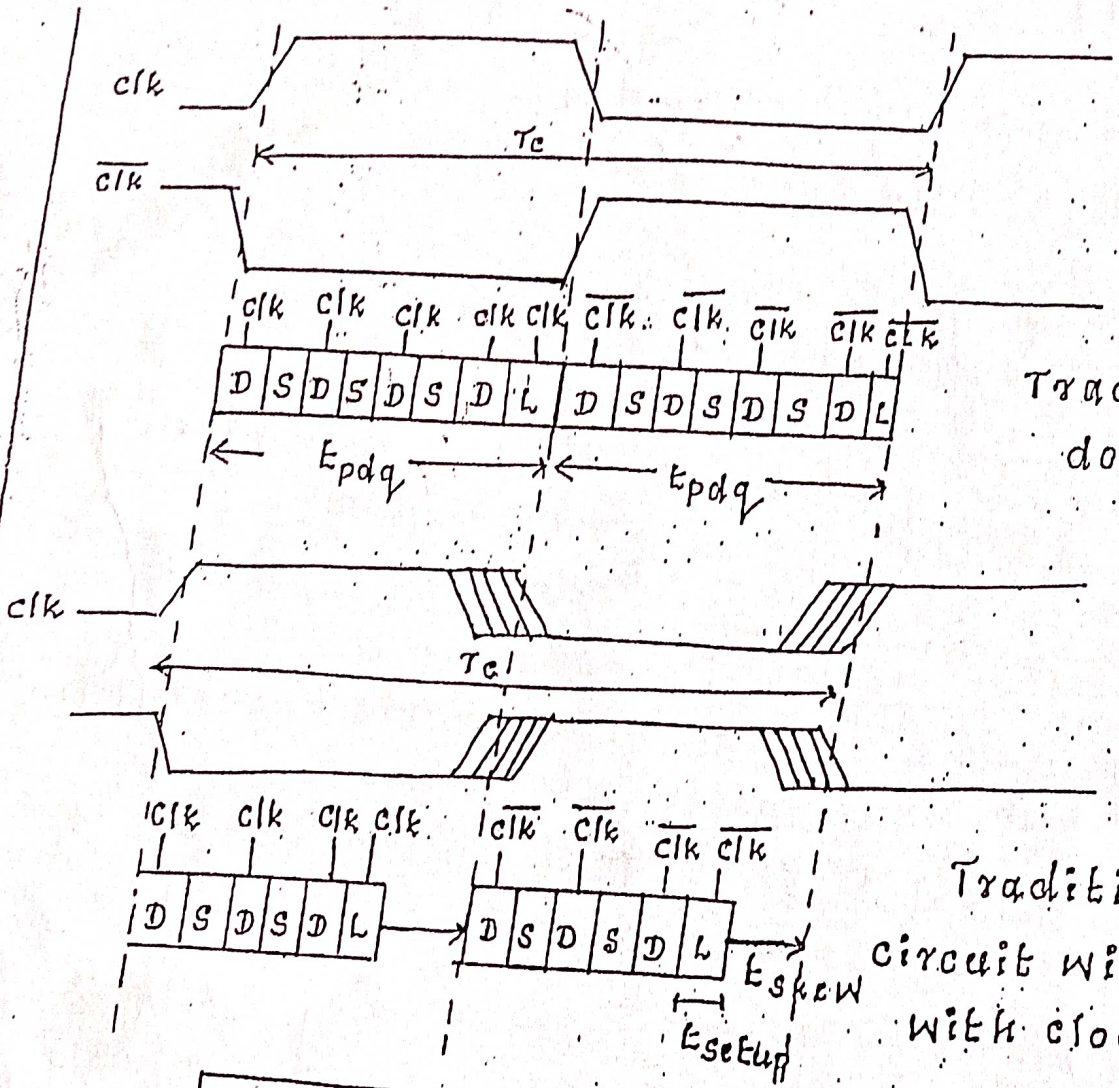
$$t_{pd} = T_c - 2t_{pdq}$$

Where, t_{pd} → Logic propagation delay

t_{pdq} = Latch D to Q propagation delay

T_c → clock period

* Traditional domino circuits have high sequencing overhead.



Traditional domino circuit

Traditional domino circuit with pipeline with clock skew

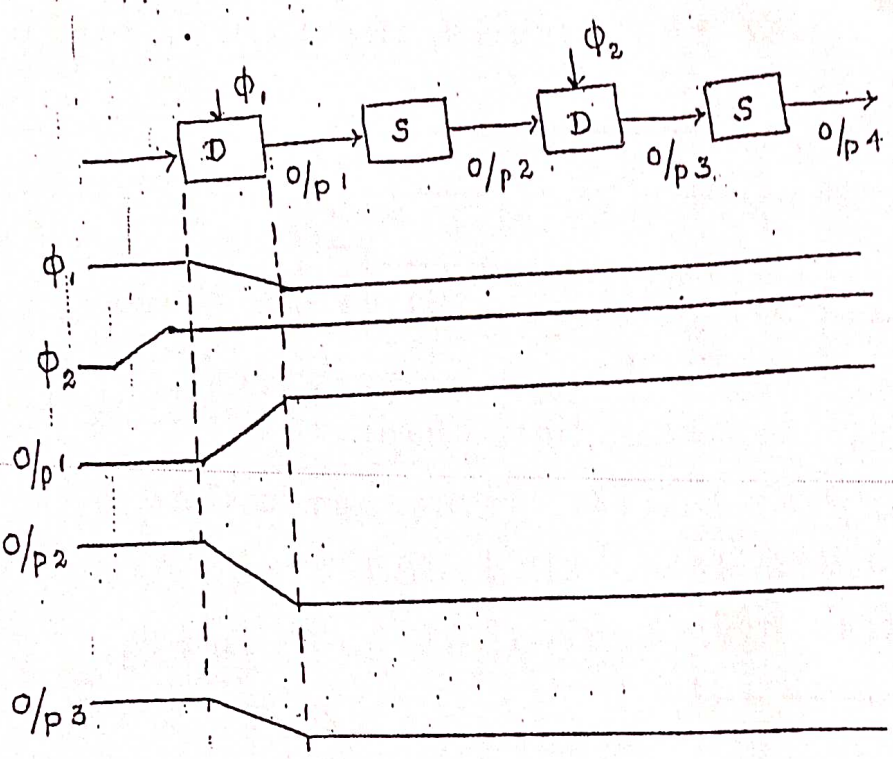
$$t_{pd} = T_c - 2t_{setup} - 2t_{skew}$$

② Skew Tolerant Domino circuits

* In this circuit, Latch is eliminated o/p 2 drives first gate in phase 2.

* The latches can be eliminated at the phase boundaries as long as the clocks overlap and dynamic gate of each phase uses a full keeper.

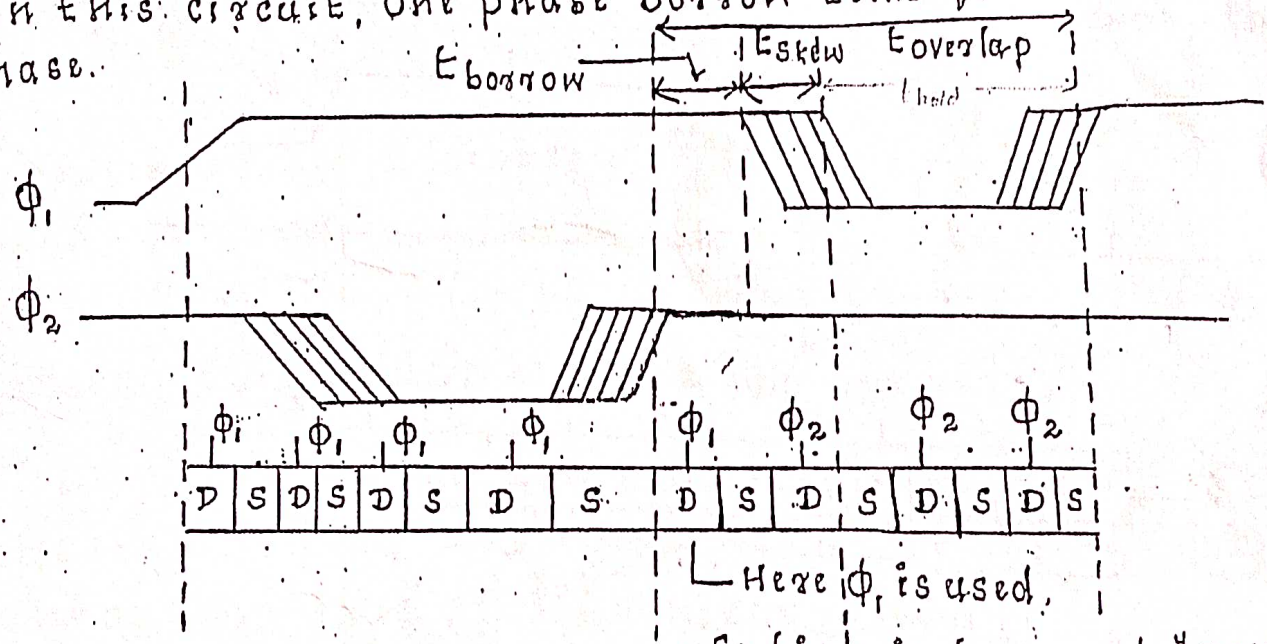
* Full keeper consists of weak cross coupled inverters to keep the output at high or Low.



D → Dynamic
S → static

③ Time borrowing in skew Tolerant Domino circuits

* In this circuit, one phase borrow time from another phase.



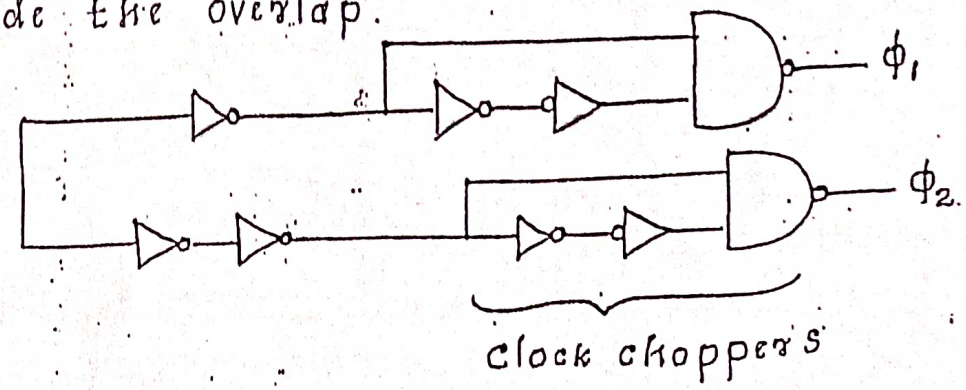
So time is borrowed from phase 1 to phase 2

$$t_{borrow} = t_{overlap} - t_{skew} = t_{hold}$$

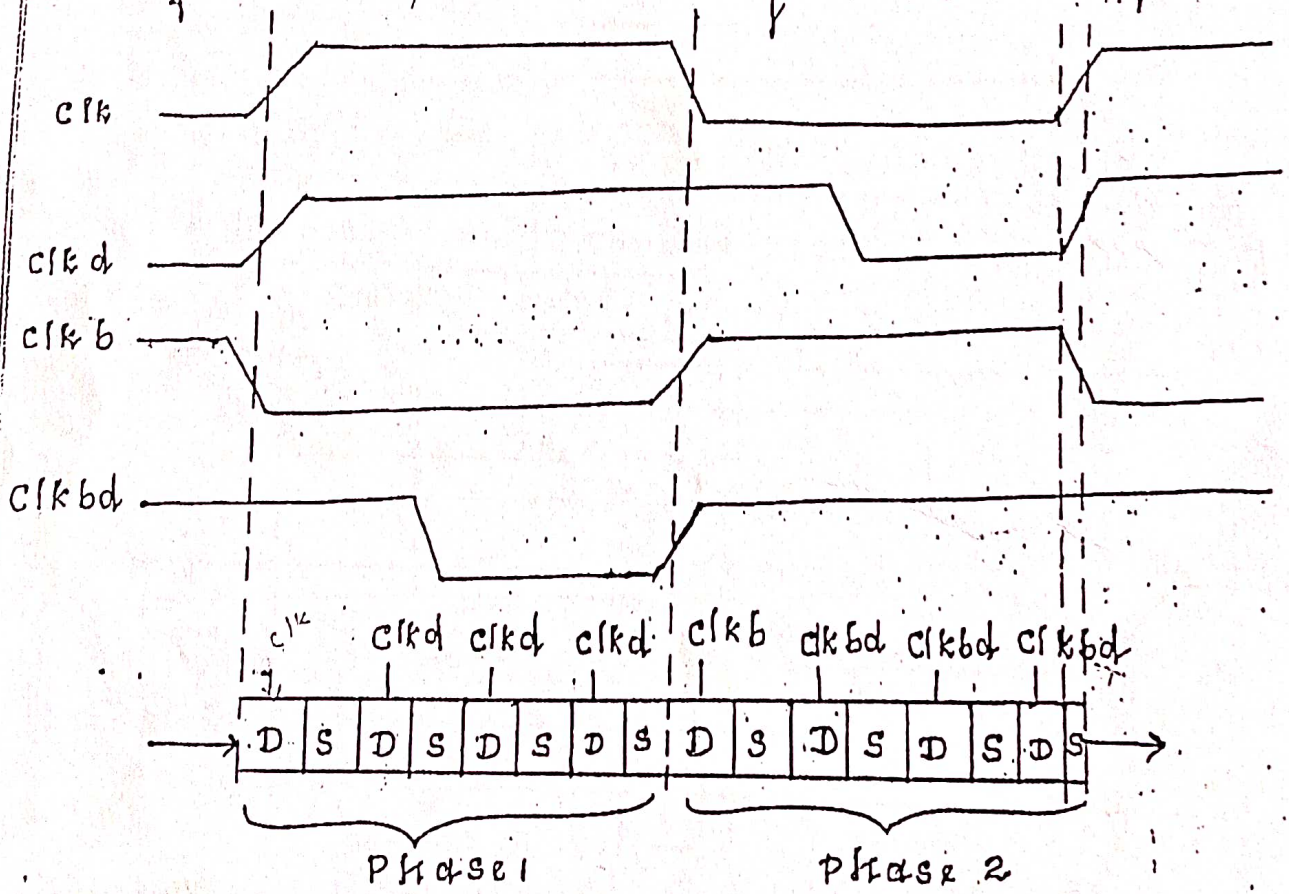
④ Two phase skew Tolerant domino and OTB Domino:

* In two phase skew tolerant domino system, the clock generator uses clock choppers. It is also known as clock stretchers.

* It is used to provide the delay in the [illegible] to provide the overlap.

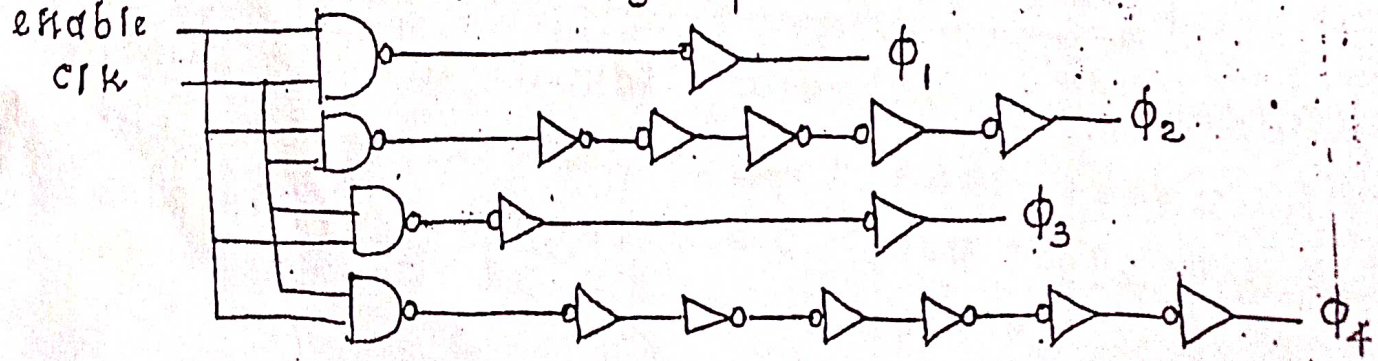


→ OTB means opportunities Time borrowing. Here clk and clkb are used. clkd and clkbd are delayed clocks, These are equivalent to ϕ_1 and ϕ_2.

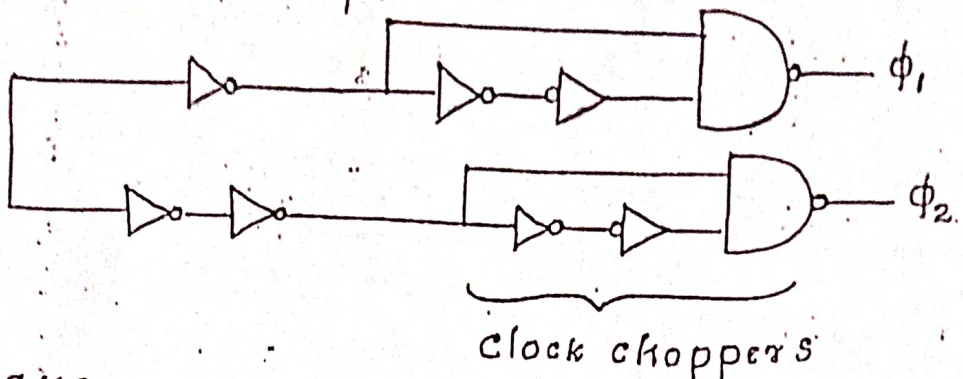


⑤ Four phase skew Tolerant domino:

* Four phases $\phi_1, \phi_2, \phi_3, \phi_4$ can be used.



* It is used to provide the delay in the falling edge to provide the overlap.



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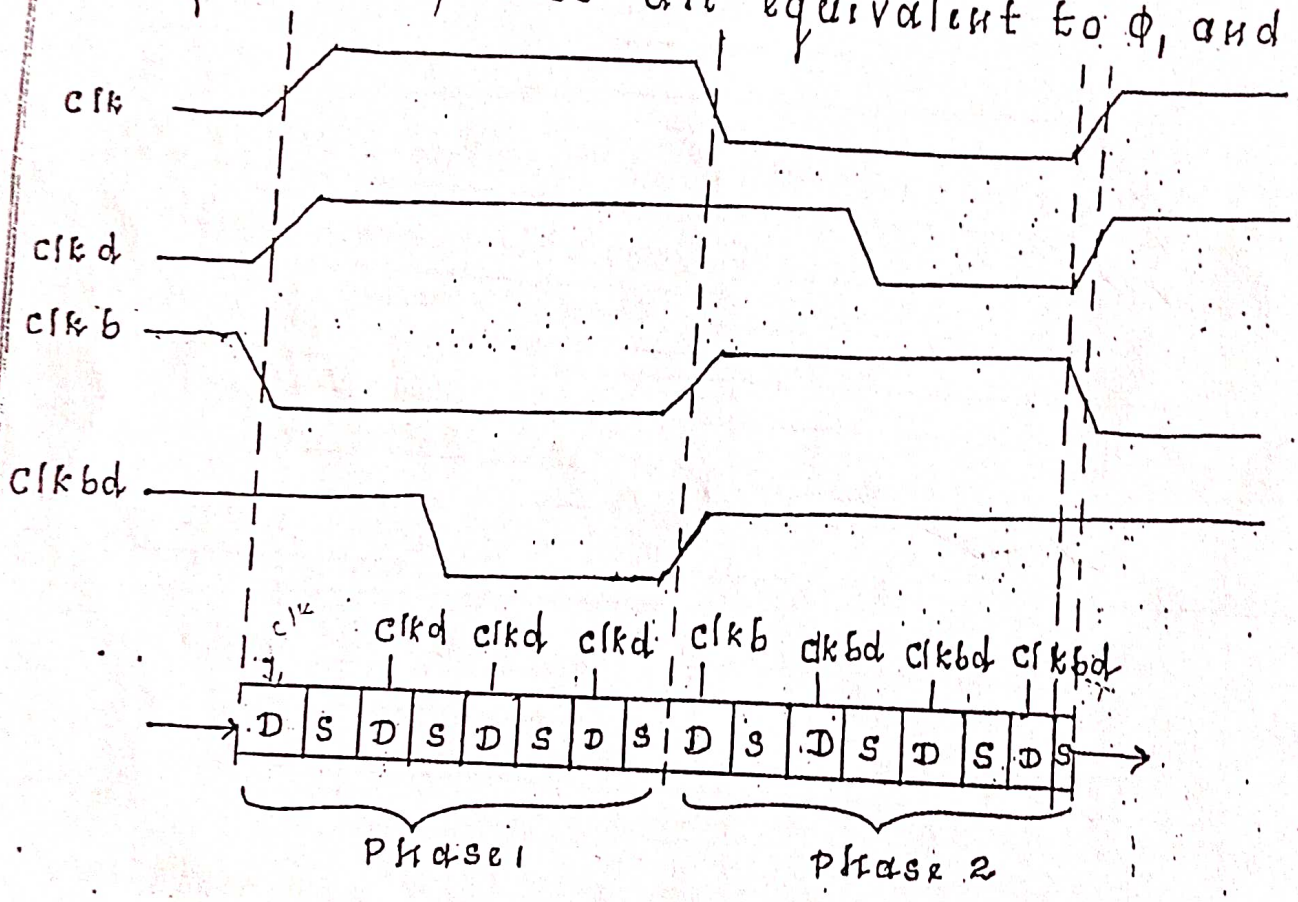

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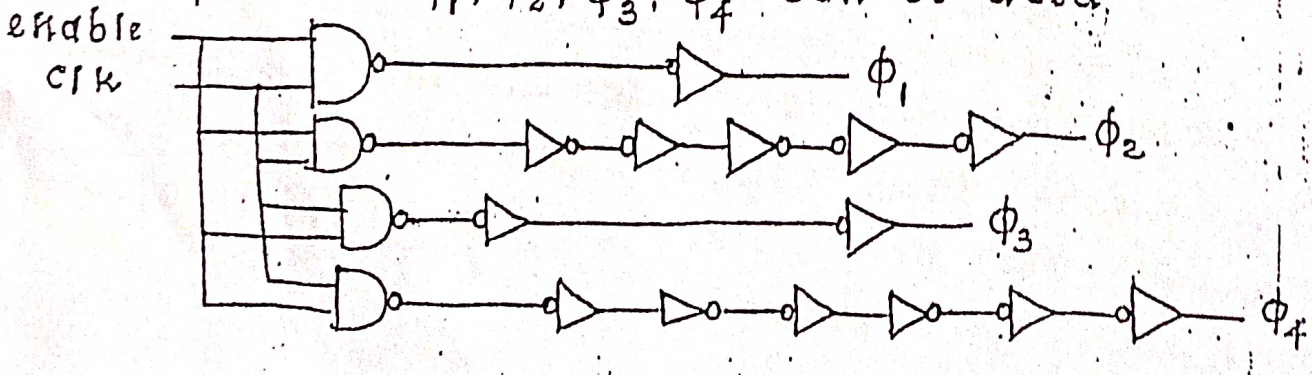
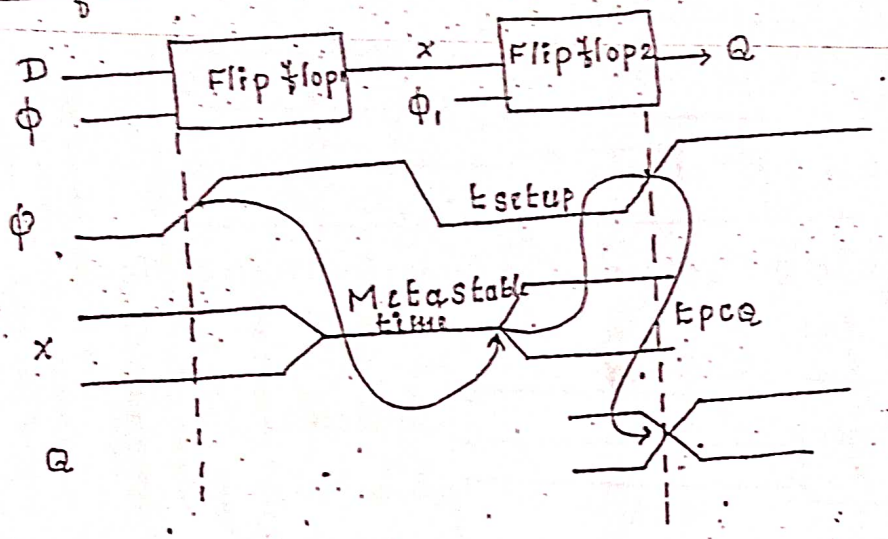


SYNCHRONIZERS

* A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an o/p aligned to the synchronizer's clock.

Simple synchronizer:



* A synchronizer accepts an i/p D and a clock ϕ. It produces an output Q.
* If the data changes the during the aperture, Q can be chosen arbitarily. If the data is stable, Q should equal D.
* Metastable state A = B = V_{TH} (V_{TH} is not a legal value) is unbounded in a synchronizer.
* F1 samples the asynchronous input D.
* output x may be meta stable some time, but settle with high probability.
* F_2 samples x and produces an o/p Q aligned with clock.
* Synchronizer has a latency of one clock cycle.

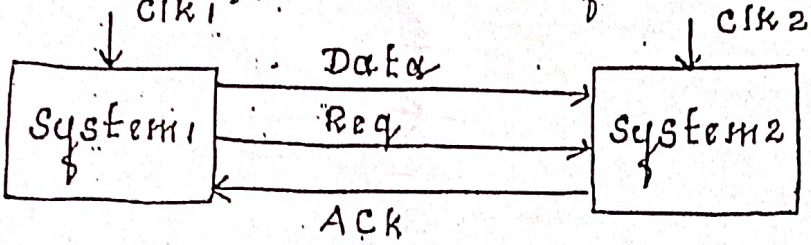
* If the synchronizer receives an average of N asynchronous input changes at D each second, the probability of synchronizer failure in any given second is,

$$P(\text{failure}) = N \cdot \frac{T_0}{T_c} \cdot e^{-\frac{(T_c - t_{setup})}{\tau_s}}$$

→ Mean time between failures

$$MTBF = \frac{1}{P_{failure}} = \frac{T_c \, e^{\frac{T_c - t_{setup}}{\tau_s}}}{N T_0}$$

② Communicating between asynchronous clock domains



* Here the relationship between clk1 and clk2 is unknown. Ack and Request signals are hand-shaking signals.

→ Common synchronizer mistakes
* usage of bad Latch
* capturing inconsistant data

③ Arbiters :-
* It decide which of the two input arrived first.
* If the spacing between the inputs exceeds some aperture time, the first i/p should be acknowledged.
* If the spacing is smaller one of the two input is acknowledge, but the choice is arbitrary.

PART – A QUESTIONS AND ANSWERS

1. What are the classification of CMOS circuit families?

- Static CMOS circuits
- Dynamic CMOS circuits
- Ratioed circuits
- Pass-transistor circuits

2. What is the characteristics of static CMOS design?

A static CMOS circuit is a combination of two networks – the pull-up network (PUN) and the pull-down network (PDN) in which at every point in time, each gate output is connected to either V_{DD} or V_{SS} via a low-resistance path.

3. List the important properties of static CMOS design.

- At any instant of time, the output of the gate is directly connected to V_{SS} and V_{DD}.
- The function of the PUN is to provide a connection between the output and V_{DD}.
- The function of the PDN is to provide a connection between the output to V_{SS}.
- Both PUN and PDN are constructed in mutually exclusive way such that one and only one of the networks is conducting in steady state. That is, the output node is always a low-impedance node in steady state.

4. What is bubble pushing?

Bubble pushing is a principle which is applied for static CMOS structure that is dual in nature that can be obtained using the duality principle of Demorgan's theorem. For example an OR gate is equivalent to a NAND gate with bubbles at its inputs and an AND gate is equivalent to a NOR gate with bubbles at its inputs.

5. What is AOI and OAI logic?

AND-OR-INVERT (AOI) logic are two-level compound (or complex) logic functions constructed from the combination of one or more AND gates followed by a NOR gate. Construction of AOI cells is particularly efficient using CMOS technology where the total number of transistor gates can be reduced compared to the same construction using NAND logic. In OR-AND-INVERT (OAI) logic where the OR gates precede an AND gate.

6. What is pin ordering?

It is a technique used to change the order of inputs in such that, the input that have frequent transition should be placed close to outputs so that delay induced in circuit can be minimized easily. Since delay varies depending on various factors such as capacitances and transistor sizes.

7. What are called asymmetric gates?

Logic gates have different logical effort for different inputs are called asymmetric gates.

8. What is unskewed gates?

For $\beta_p = \beta_n$, the inverter threshold voltage V_{inv} is $V_{DD}/2$. This maximizes noise margins and allows a capacitive load to charge and discharge in equal times by providing equal current source and sink capabilities is called unskewed gates.

9. What is skewed gates?

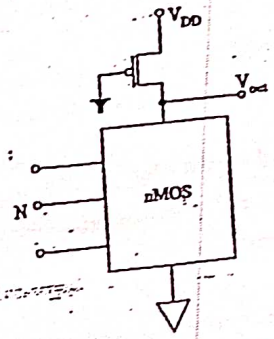
Gates with different beta ratios β_p/β_n are called skewed gates. If $\beta_p/\beta_n > 1$, the gate is H-skewed. If $\beta_p/\beta_n < 1$, the gate is Low-skewed. If $\beta_p/\beta_n = 1$, the gate is unskewed.

10. What is ratioed circuits?

Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, often at the cost of reduced robustness and extra power dissipation.

11. What is pseudo-nMOS circuits?

Circuit implemented with nMOS having grounded pMOS gate is called pseudo-nMOS circuits.



12. What are the advantages of psuedo-nMOS circuits?

1. Reduce number of transistors ($N+1$, versus $2N$ for CMOS)
2. The normal high output voltage (V_{OH}) for this gate is V_{DD} since the pull-down stack are turned off when the output is pulled high.
3. Pseudo-nMOS gates offer improve speed factor.

13. What are the disadvantages of pseudo-nMOS circuits?

1. Reduced noise margin
2. Static power dissipation

14. What is Ganged CMOS circuit?

Ganged CMOS also called as symmetric circuits. They are constructed with pair of inverters ganged together to perform a function.

15. What is SFPL?

Source-Follower pull-up logic is a variation on Psuedo-nMOS whereby the load device is an N pull-down transistor and N source-follower pull-ups are used on the inputs.

16. What is CVSL?

Cascade voltage switch logic (CVSL) belongs to class of differential-logic types. The network consists of a dual n-block instead of a dual p-block and a pair of cross-coupled pMOS transistors compute the logic function and its complement. CVSL can be roughly as fast as dynamic logic, it dissipates almost as little static power as static CMOS and is relatively robust against large structure.

17. What are the characteristics of CVSL?

1. CVSL is a differential type of logic circuit whereby both true and complement inputs are required.
2. N pull-down trees are the dual of each other.
3. P pull-up devices are cross-coupled to latch output.
4. Both true and complement outputs are obtained.

18. What is Dynamic CMOS logic?

Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.

- Requires only $N+2$ transistors
- Takes a sequence of precharge and conditional evaluation phases to realize logic functions.

19. What are the properties of Dynamic logic?

1. Logic function is implemented by the pull-down network only.
2. Full swing outputs (V_{OL} = GND and $V_{OH} = V_{DD}$).
3. Non-ratioed.
4. Faster switching speeds.
5. Needs a precharge clock.

20. What is precharge phase?

The input to the next stage is charged up through the pMOS transistor when the clock is low, this phase of the clock is known as the precharge phase.

21. What is Evaluation phase?

When the clock is high however, the pMOS is cutoff and the bottom nMOS is turned ON, thereby disconnecting the output node from V_{DD} and providing a possible pull-down path to ground through the bottom nMOS transistor. This part of the clock cycle is known as the evaluation phase.

22. What is footed and unfooted dynamic circuits?

In unfooted dynamic circuits uses only one pMOS through which a clk is connected which give rise to contention problem when both pMOS and nMOS ON precharge phase.

In footed dynamic circuits uses a single pMOS precharge transistor and one nMOS evaluation transistors to avoid contention problem.

23. What are the disadvantages of dynamic CMOS logic?

1. A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate.
2. Violate monotonicity during evaluation phase.

24. What is CMOS Domino logic?

A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS domino logic.

25. What are the properties of domino logic?

1. Only non-inverting logic can be implemented.
2. Very high speed having $t_{pHL} = 0$
3. Eliminates the monotonicity problem.

26. What is Dual-rail domino logic

A circuit is said to be Dual-rail domino if each logical variable is represented by two wires, one that goes high if the signal is false, with this encoding, an input variable going true can cause an output variable to go true or false.

27. What are called sequencing elements?

Flip-flops or latches are memory elements, that hold data called tokens. These memory elements are used to 'sequence' data (ie) make a large amount of data appear in a predetermined bit by bit sequence, they are called as sequencing elements.

28. What is called sequencing overhead?

Sequencing elements delay tokens that arrive too early, preventing them from catching up with the previous tokens unfortunately, they inevitably add some delay to tokens that are already critical, decreasing the performance of the system. This extra delay is called sequencing overhead.

29. What is called static and dynamic sequencing element?

A sequencing element with static storage employs some sort of feedback to retain its output value indefinitely.

A sequencing element with dynamic storage generally maintains its value as charge on a capacitor that will leak away if not refreshed for a long period of time.

30. List the methods of sequencing static circuits.

The three most widely used methods of sequencing static circuits

(i) Flip-flops

(ii) 2-Phase transparent latches

(iii) Pulsed latches

31. What is called pulsed latch?

The latch that has short clock-to-Q delay and a long hold time is called pulsed latch or single-phase level triggered latch.

32. Define propagation delay.

Upper bound on interval between valid inputs and valid outputs (or) the required interval times to change the output after applying the input signal is called propagation delay.

33. Define contamination delay.

It is the lower bound on interval between invalid inputs and invalid output is called the contamination delay.

34. Define clock-to-Q propagation delay.

(i) Propagation delay t_{PLH} is measured from the 50% triggering edge point of the clock pulse to the 50% transition of the output from low to high

(ii) Propagation delay t_{PHL} is measured from the 50% triggering edge of the clock pulse to the high to low transition of the output.

35. Define clock-to-Q contamination delay.

Output signal start to change after its input change and settles to the final value within propagation delay is called clock-to-Q contamination delay.

36. Define setup time

The time before the clock edge that the D input has to be stable is called setup time.

37. Define hold time

The time after the clock edge that the D input remain stable is called hold time.

38. Define setup time failure or max-delay failure.

If the combinational logic delay is too long, the receiving element will miss its setup time and sample the wrong value. This is called a setup time failure or max-delay failure.

39. Define time borrowing or cycle stealing.

The ability of slow logic in one half-cycle to use time nominally allocated to faster logic in another half-cycle is called time borrowing or cycle stealing.

40. What is charge keeper circuit?

The domino cascade suffer from charge leakage on the dynamic nodes. If a dynamic node is precharged high and then left floating, the voltage on the dynamic node will drift over time due to subthreshold and junction leakage. Charge-keeper circuit eliminate this problem and retain the charge till next precharge condition.

41. What is MODL?

Multiple-output domino logic (MODL) is a variation of standard domino logic that accepts multiple inputs and can produce two or more distinct output functions.

42. What is NP and zipper domino logic?

An alternative to Domino logic is NORA, or Domino-zipper logic. NORA stands for 'no-race' indicating another method to eliminate the 'racing' problem of directly cascaded dynamic logic blocks.

43. What is CMOSTG?

CMOS transmission gate implemented with two styles conjunction with transmission gate and static CMOS to improve performance.

44. What is CPL?

The main concept behind complementary pass transistor logic (CPL) is the use of only an nMOS network for the implementation of logic functions. It consists of nMOS pass transistor logic network driven by two sets of complementary inputs and CMOS inverter used as buffers.

45. What is clock skew?

In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation is called clock skew.

46. What is pulsed latch?

Pulsed latch consisting of the set of pass gates that define the transparency window, buffer inverters, and weak feedback path to keep the value stored in the PL output at the end of transparency window.

47. What is resettable latch?

Resettable latches and flip-flops employes a control input called reset signal to enter a known initial state on startup.

48. What are the two types of reset?

The two types of reset are

1. Synchronous
2. Asynchronous

In synchronous reset, the flip flop changes with synchronous control inputs and clock signal.

In asynchronous reset, the output is independent of the synchronous input and the clock input.

49. What is klass semidynamic flip-flop?

It is a single-input single-output positive edge-triggered flip-flop. It is domino-style fast and allows for efficient embedded combinational logic and reduces the load on the data network.

50. What is Differential flip-flops?

Differential flip-flops accept true and complementary inputs and produce true and complementary outputs. They are built from a clocked sense amplifier so they can rapidly respond to small differential input voltages.

51. What is TSPC?

The true-single-phase-clock latch is constructed by merging CMOS Domino and CMOS NORA logic. Conventional latches require both true and complementary clock signals. Normally the complementary signals are generated with an inverter in the latch cell.

52. What is synchronizers?

A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer's clock. Because the input can change during the synchronizer's aperture, the synchronizer has a non zero probability of producing a metastable output.

53. What is metastability?

Flip-flop is a device that is susceptible to metastability. It has two well-defined stable states, traditionally designated 0 and 1, but under certain conditions it can hover between them for longer than a clock cycle. This condition is known as metastability.

54. What is metastable state?

In reality, when a flip-flop samples as input that is changing during its aperture, the output may momentarily take on a voltage between 0 and V_{DD} that is in the forbidden zone. This is called a metastable state.

55. What is Arbiter?

An arbiter is a circuit designed to determine which of several signals arrive first. Arbiters are used in asynchronous circuits to order computational activities for shared resources to prevent concurrent incorrect operations.

56. What is Arbitration?

A closely related problem to synchronization is arbitration. Arbitration is necessary when two or more modulus would like exclusive access to a shared resource.

Part-A

Draw a pseudo NMOS inverter (Nov 2011)

Enumerate the features of synchronizers (May 2013)

Part-B

Describe the basic principle of operation of dynamic CMOS, domino and NP domino logic with neat diagrams (Nov 2011)

Draw and explain the operation of conventional CMOS pulsed and resettable latches.

Write a brief note on sequencing dynamic circuits (Nov 2012)

Discuss the techniques to reduce switching activity in a static and dynamic CMOS circuits (May 2013).